5

MOS Capacitor

CHAPTER OBJECTIVES

This chapter builds a deep understanding of the modern MOS (metal–oxide–semiconductor) structures. The key topics are the concepts of surface depletion, threshold, and inversion; MOS capacitor C–V; gate depletion; inversion-layer thickness; and two imaging devices—charge-coupled device and CMOS (complementary MOS) imager. This chapter builds the foundation for understanding the MOSFETs (MOS Field-Effect Transistors).

The acronym **MOS** stands for **metal–oxide–semiconductor**. An MOS capacitor (Fig. 5–1) is made of a semiconductor body or substrate, an insulator film, such as SiO_2, and a metal electrode called a **gate**. The oxide film can be as thin as 1.5 nm. One nanometer is equal to 10 Å, or the size of a few oxide molecules.

Before 1970, the gate was typically made of metals such as Al (hence the M in MOS). After 1970, heavily doped polycrystalline silicon (see the sidebar, Three Kinds of Solid, in Section 3.7) has been the standard gate material because of its ability to

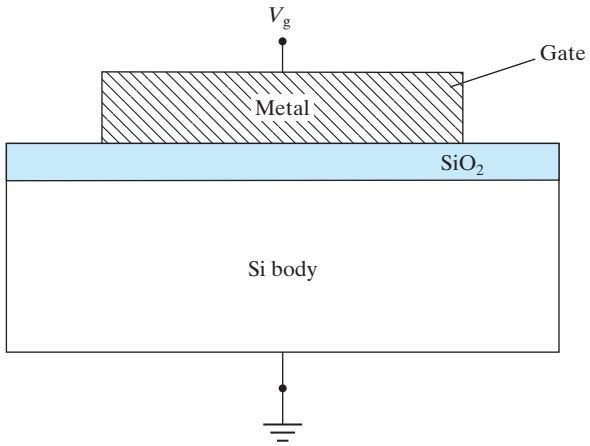

FIGURE 5–1 The MOS capacitor.

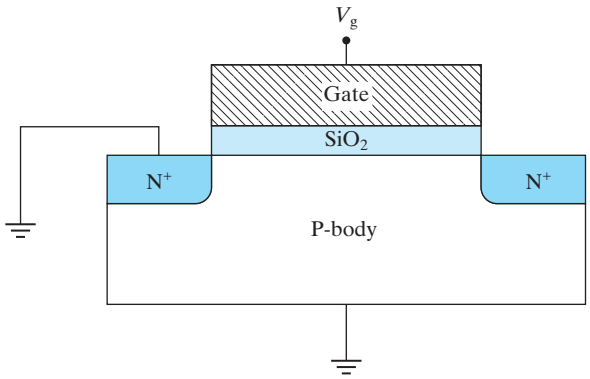

FIGURE 5–2 An MOS transistor is an MOS capacitor with PN junctions at two ends.

withstand high temperature without reacting with SiO_2. But the MOS name stuck. Unless specified otherwise, you may assume that the gate is made of heavily doped, highly conductive, polycrystalline silicon, or poly-Si for short. After 2008, the trend is to reintroduce metal gate and replace SiO_2 with more advanced dielectrics for the most advanced transistors (see Section 7.4).

The MOS capacitor is not a widely used device *in itself*. However, it is part of the MOS transistor—the topic of the next two chapters. The MOS transistor is by far the most widely used semiconductor device. An MOS transistor (Fig. 5–2) is an MOS capacitor with two PN junctions flanking the capacitor. This transistor structure is often a better structure for studying the MOS *capacitor* properties than the MOS capacitor itself as explained in Section 5.5.

5.1 • FLAT-BAND CONDITION AND FLAT-BAND VOLTAGE •

It is common to draw the energy band diagram with the oxide in the middle and the gate and the body on the left- and right-hand sides as shown in Fig. 5–3. The band diagram for $V_g = 0$ (Fig. 5–3b) is quite complex.

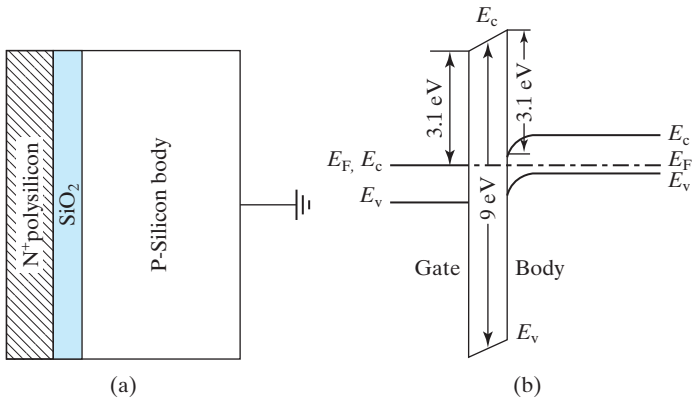

FIGURE 5–3 (a) Polysilicon-gate/oxide/semiconductor capacitor and (b) its energy band diagram with no applied voltage.

It is a good strategy to first study the energy band diagram for a special bias condition called the **flat-band condition**. Flat band is the condition where the energy band (E_c and E_v) of the substrate is flat at the Si–SiO_2 interface as shown in Fig. 5–4. This condition is achieved by applying a negative voltage to the gate in Fig. 5–3b, thus raising the band diagram on the left-hand side. (See Section 2.4 for the relation between voltage and the band diagram.) When the band is flat in the body as in Fig. 5–4, the surface electric field in the substrate is zero. Therefore the electric field in the oxide is also zero[1], i.e., E_c and E_v of SiO_2 are flat, too. E_c and E_v of SiO_2 are separated by 9 eV, the E_g of SiO_2. E_0, the **vacuum level**, is the energy state of electrons outside the material. E_0 of SiO_2 is above E_c by 0.95 eV. The difference between E_0 and E_c is called the **electron affinity**, another material parameter just as E_g is a material parameter. Si has an electron affinity equal to 4.05 eV. E_0 must be continuous at the Si–SiO_2 interface as shown in Fig. 5–4 (otherwise the electric field would be infinite). Therefore, E_c of SiO_2 is 3.1 eV higher than E_c of Si. This 3.1 eV is the Si–SiO_2 **electron energy barrier**. The **hole energy barrier** is 4.8 eV in Fig. 5–4. Because of these large energy barriers, electrons and holes normally cannot pass through the SiO_2 gate dielectric. E_c in the poly-silicon gate is also lower than the E_c of SiO_2 by 3.1 eV (the Si–SiO_2 energy barrier). Finally, E_F of the N^+poly-Si may be assumed to coincide with E_c for simplicity. In SiO_2, the exact position of E_F has no significance. If we place E_F anywhere around the middle of the SiO_2 band gap,

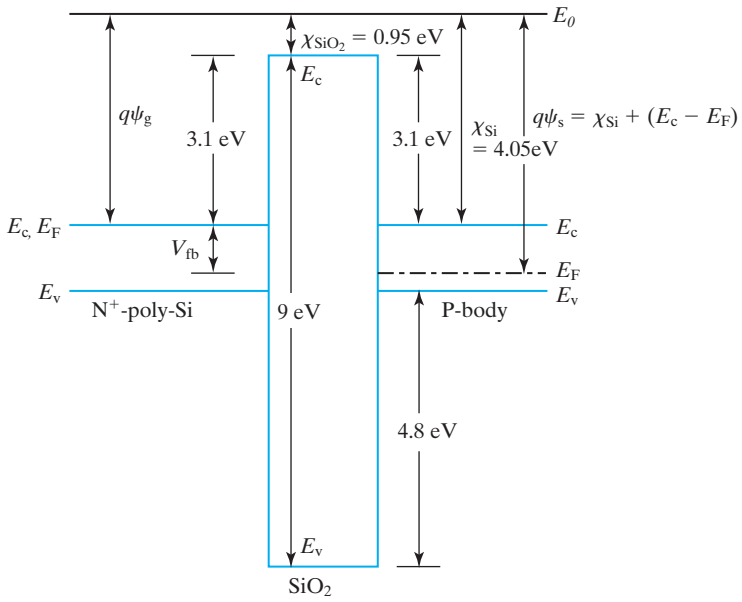

FIGURE 5–4 Energy band diagram of the MOS system at the flat-band condition. A voltage equal to V_{fb} is applied between the N^+-poly-Si gate and the P-silicon body to achieve this condition. ψ_g is the gate-material work function, and ψ_s is the semiconductor work function. E_0 is the vacuum level.

[1] According to Gauss's Law, with no interface charge, $\varepsilon_s \mathscr{E}_s = \varepsilon_{ox}\mathscr{E}_{ox}$ where $\mathscr{E}_s$ and $\mathscr{E}_{ox}$ are the body surface field and the oxide field.

$n = N_c\exp[(E_c - E_F)/kT]$ would be a meaninglessly small number such as 10^{-60} cm^{-3}. Therefore, the position of E_F in SiO_2 is immaterial.

The applied voltage at the flat-band condition, called V_{fb}, the **flat-band voltage**, is the difference between the Fermi levels at the two terminals.

$$V_{fb} = \psi_g - \psi_s \tag{5.1.1}$$

ψ_g and ψ_s are the gate work function and the semiconductor work function, respectively, in volts. The work function is the difference between E_0 and E_F. For an N^+-poly-Si gate, $\psi_g = 4.05$ V.[2] For the P-Si body, $\psi_s = 4.05\text{ V} + (E_c - E_F)/q$. For the example at hand, Eq. (5.1.1) and Fig. 5–4 indicate a negative V_{fb}, about –0.7 V.

5.2 • SURFACE ACCUMULATION •

How would Fig. 5–4 change if a more negative V_g than V_{fb} is applied? The band diagram on the gate side would be pushed upward (see Section 2.4). The result is shown in Fig. 5–5. Note that Fig. 5–5 is not drawn to scale (e.g., 3.1 eV is not about three times the silicon band gap) for the economy of page space. Such not-to-scale drawings are the norm. When $V_g \neq V_{fb}$, ϕ_s (surface voltage) and V_{ox} (oxide voltage) will be non-zero in general. $q\phi_s$ is the band bending in the substrate. Because the substrate is the voltage reference, ϕ_s is negative if E_c bends upward toward the surface as shown in Fig. 5–5 and positive if E_c bends downward. If this discussion of the sign of ϕ_s sounds strange, please review Sec. 2.4. V_{ox} is the voltage across the oxide. Again, V_{ox} is negative if the SiO_2 energy band tilts up toward the gate as it does in Fig. 5–5, and positive if it tilts downward toward the gate.

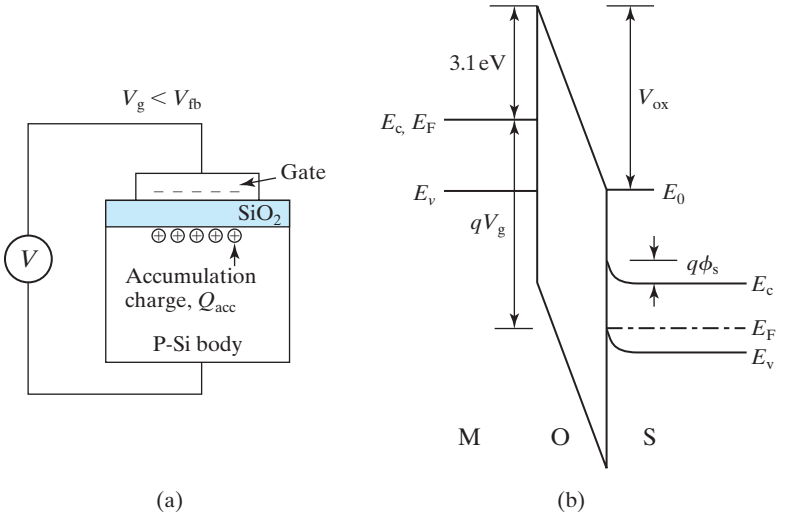

FIGURE 5–5 This MOS capacitor is biased into surface accumulation ($p_s > p_0 = N_a$). (a) Types of charge present. ⊕ represents holes and – represents negative charge. (b) Energy band diagram.

[2] In this case, ψ_g happens to be equal to χ_{Si}. In general, ψ_g is defined as the difference between E_0 and E_F.

Because E_v is closer to E_F at the surface than in the bulk, the surface hole concentration, p_s, is larger than the bulk hole concentration, $p_0 = N_a$. Specifically,

$$p_s = N_a e^{-q\phi_s/kT} \tag{5.2.1}$$

Since ϕ_s may be –100 or –200 mV, $p_s >> N_a$. That is to say, there are a large number of holes at or near the surface. They form an **accumulation layer** and these holes are called the **accumulation-layer holes**, and their charge the **accumulation charge, Q_{acc}**. This condition is known as **surface accumulation**. If the substrate were N type, the accumulation layer would hold electrons.

A relationship that we will use again and again is

$$\boxed{V_g = V_{fb} + \phi_s + V_{ox}} \tag{5.2.2}$$

At flat band, $V_g = V_{fb}$, $\phi_s = V_{ox} = 0$ and Eq. (5.2.2) is satisfied. If $V_g \neq V_{fb}$, the difference must be picked up by ϕ_s and V_{ox}. In the case of surface accumulation, ϕ_s may be ignored in a first-order model since it is quite small and Eq. (5.2.2) becomes

$$V_{ox} = V_g - V_{fb} \tag{5.2.3}$$

Using Gauss's Law, $\mathscr{E}_{ox} = -\dfrac{Q_{acc}}{\varepsilon_{ox}}$

$$V_{ox} = \mathscr{E}_{ox} T_{ox} = -\frac{Q_{acc}}{C_{ox}} \tag{5.2.4}$$

where C_{ox} is the oxide capacitance per unit area (F/cm^2) and Q_{acc} is the accumulation charge (C/cm^2). Equation (5.2.4) is the usual capacitor relationship, $V = Q/C$ (or $Q = C$–V) except for the negative sign. In $V = Q/C$, the capacitor voltage and charge are both taken from the same electrode. In the MOS capacitor theory, the voltage is the gate voltage, but the charge is the substrate charge because interesting things happen in the substrate. This unusual choice leads to the negative sign in Eq. (5.2.4). Equations (5.2.4) and (5.2.3) tell us

$$Q_{acc} = -C_{ox}(V_g - V_{fb}) \tag{5.2.5}$$

Therefore, the MOS capacitor in accumulation behaves like a capacitor with $Q = C$–V (or $-C$–V as explained earlier) but with a shift in V by V_{fb}. The shift is easily understandable because $Q_{acc} = 0$ when $V_g = V_{fb}$. In general, Eq. (5.2.4) should read

$$\boxed{V_{ox} = -Q_{sub}/C_{ox}} \tag{5.2.6}$$

where Q_{sub} is all the charge that may be present in the substrate, including Q_{acc}.

5.3 • SURFACE DEPLETION •

How would Fig. 5–4 change if a more positive V_g than V_{fb} is applied? The band diagram on the gate side will be pulled downward as shown in Fig. 5–6b. Clearly, *there is now a depletion region at the surface* because E_F is far from both E_c and E_v

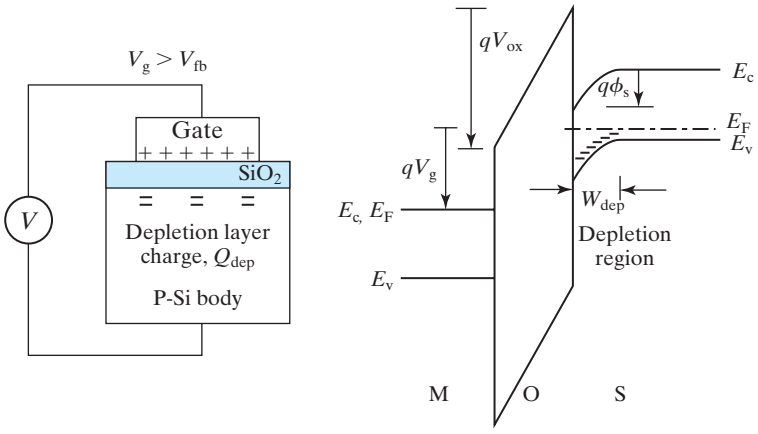

FIGURE 5–6 This MOS capacitor is biased into surface depletion. (a) Types of charge present; (b) energy band diagram.

and electron and hole densities are both small. This condition is called **surface depletion**. The depletion region has a width, W_{dep}. Equation (5.2.6) becomes

$$V_{ox} = -\frac{Q_{sub}}{C_{ox}} = -\frac{Q_{dep}}{C_{ox}} = \frac{qN_aW_{dep}}{C_{ox}} = \frac{\sqrt{qN_a2\varepsilon_s\phi_s}}{C_{ox}} \tag{5.3.1}$$

$$\phi_s = \frac{qN_aW_{dep}^2}{2\varepsilon_s} \tag{5.3.2}$$

Q_{dep} is negative because the acceptor ions (after accepting the extra electrons) are negatively charged. In Eqs. (5.3.1) and (5.3.2), we used $W_{dep} = \sqrt{(2\varepsilon_s\phi_s)/(qN_a)}$ [Eq. (4.2.10)]. Combining Eqs. (5.3.1), (5.3.2), and (5.2.2),

$$V_g = V_{fb} + \phi_s + V_{ox} = V_{fb} + \frac{qN_aW_{dep}^2}{2\varepsilon_s} + \frac{qN_aW_{dep}}{C_{ox}} \tag{5.3.3}$$

This equation can be solved to yield W_{dep} as a function of V_g. With W_{dep} determined, V_{ox} [Eq. (5.3.1)] and ϕ_s [Eq. (5.3.2)] become known.

5.4 • THRESHOLD CONDITION AND THRESHOLD VOLTAGE •

Let's make V_g in Fig. 5–6 increasingly more positive. This bends the energy band down further. At some V_g, E_F will be close enough to E_c at the Si–SiO_2 interface that the surface is no longer in depletion but at the **threshold** of **inversion**. The term inversion means that the surface is inverted from P type to N type, or electron rich. Threshold is often defined as the condition when the surface electron concentration, n_s, is equal to the bulk doping concentration, N_a. That means $(E_c - E_F)_{surface} = (E_F - E_v)_{bulk}$, or $A = B$ in Fig. 5–7.[3] That, in turn, means

[3] Assuming $N_c = N_v$, we conclude that $A = B$ when $n_s = N_a$.

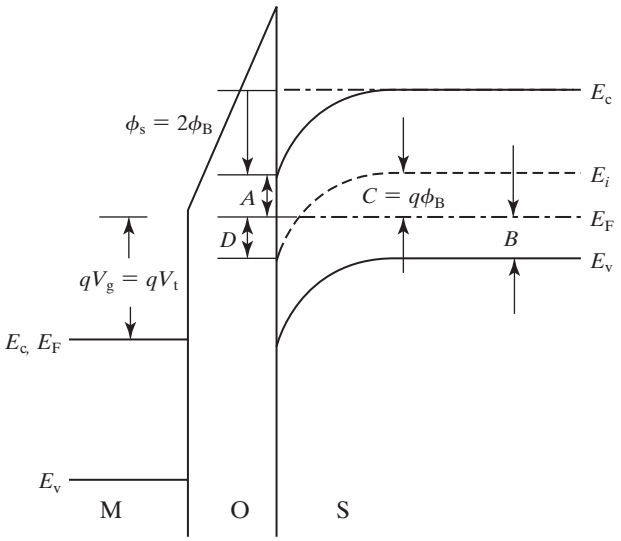

FIGURE 5–7 The threshold condition is reached when $n_s = N_a$, or equivalently, $A = B$, or $\phi_s = \phi_{st} = 2\phi_B$. Note that positive ϕ_{st} corresponds to downward band bending.

$C = D$. E_i is a curve drawn at **midgap**, which is half way between E_c and E_v. Let the surface potential (band bending) at the threshold condition be ϕ_{st}. It is equal to $(C + D)/q = 2C/q = 2\phi_B$.

Using Eqs. (1.8.12) and (1.8.8) and assuming $N_c = N_v$,

$$q\phi_B \equiv \frac{E_g}{2} - (E_F - E_v)\Big|_{bulk}$$
$$= kT\ln\frac{N_v}{n_i} - kT\ln\frac{N_v}{N_a} = kT\ln\frac{N_a}{n_i} \tag{5.4.1}$$

ϕ_s at the threshold condition is

$$\boxed{\phi_{st} = 2\phi_B = 2\frac{kT}{q}\ln\frac{N_a}{n_i}} \tag{5.4.2}$$

The V_g at the threshold condition is called the **threshold voltage**, V_t. Substituting Eqs. (5.4.2) and (5.3.1) into Eq. (5.2.2),

$$\boxed{V_t = V_{fb} + 2\phi_B + \frac{\sqrt{qN_a 2\varepsilon_s 2\phi_B}}{C_{ox}}} \tag{5.4.3}$$

The threshold voltage as a function of T_{ox} and body doping using Eq. (5.4.3) is plotted in Fig. 5–8. In this figure, the gate dielectric is assumed to be SiO_2 with dielectric constant $\varepsilon_{ox} = 3.9$.

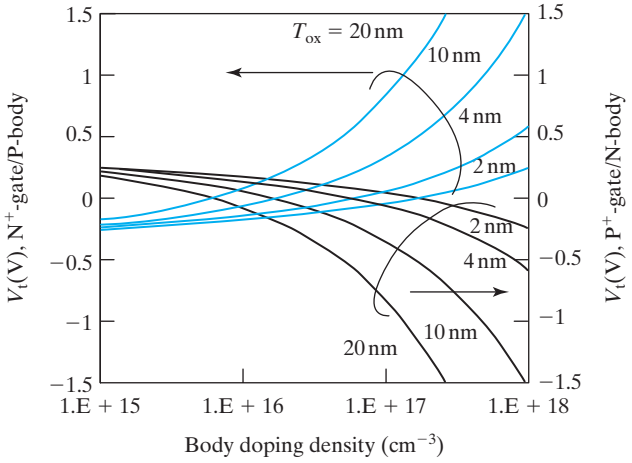

FIGURE 5–8 Theoretical threshold voltage vs. body doping concentration using Eq. (5.4.3). See Section 5.5.1 for a discussion of the gate doping type.

• N-Type Body •

For an N-type body, Eq. (5.4.3) becomes

$$V_t = V_{fb} + \phi_{st} - \frac{\sqrt{2qN_d\varepsilon_s|\phi_{st}|}}{C_{ox}} \tag{5.4.4}$$

$$\phi_{st} = -2\phi_B \tag{5.4.5}$$

$$\phi_B = \frac{kT}{q}\ln\frac{N_d}{n_i} \tag{5.4.6}$$

Exercise: Draw the band diagram of an N-body MOS capacitor at threshold and show that the second term (ϕ_{st}) and the third term (V_{ox}) in Eq. (5.4.4) are negative.

5.5 • STRONG INVERSION BEYOND THRESHOLD •

Figure 5–9b shows the energy diagram at strong inversion, $V_g > V_t$. As shown in Fig. 5–9a, there is now an **inversion layer**, which is filled with **inversion electrons.** The **inversion charge density** is represented with Q_{inv} (C/cm^2). ϕ_s does not increase much further beyond $2\phi_B$ since even a 0.1 V further increase in ϕ_s would induce a much larger surface electron density and therefore a larger V_{ox} that would soak up the V_g in Eq. (5.2.2). If ϕ_s does not increase, neither will the depletion region width. Approximately speaking, W_{dep} has reached its maximum value

$$W_{dmax} = \sqrt{\frac{2\varepsilon_s 2\phi_B}{qN_a}} \tag{5.5.1}$$

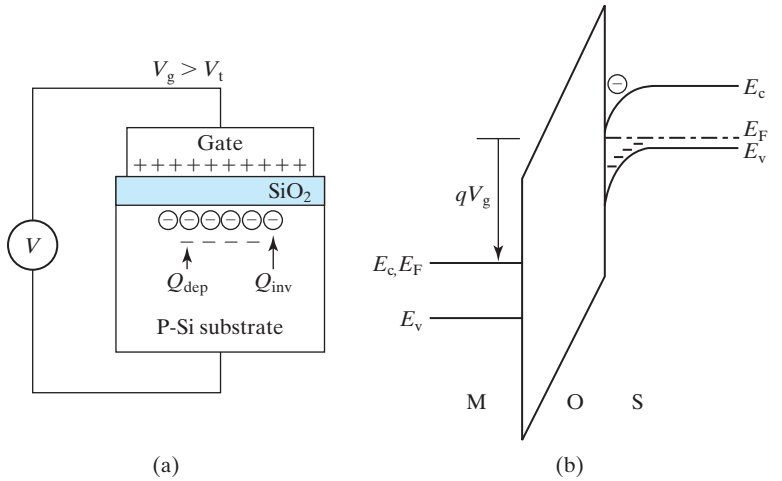

FIGURE 5–9 An MOS capacitor biased into inversion. (a) Types of charge present; (b) energy band diagram with arrow indicating the sense of positive V_g.

$$V_g = V_{fb} + 2\phi_B - \frac{Q_{dep}}{C_{ox}} - \frac{Q_{inv}}{C_{ox}} = V_{fb} + 2\phi_B + \frac{\sqrt{qN_a 2\varepsilon_s 2\phi_B}}{C_{ox}} - \frac{Q_{inv}}{C_{ox}}$$

$$= V_t - \frac{Q_{inv}}{C_{ox}} \tag{5.5.2}$$

Equations (5.2.2) and (5.2.6) are used in deriving Eq. (5.5.2).

$$\therefore \quad \boxed{Q_{inv} = -C_{ox}(V_g - V_t)} \tag{5.5.3}$$

Equation (5.5.3) confirms that the MOS capacitor in strong inversion behaves like a capacitor except for a voltage offset of V_t. At $V_g = V_t$, $Q_{inv} = 0$.

In this section, we have assumed that electrons will appear in the inversion layer whenever the closeness between E_c and E_F suggests their presence. However, there are few electrons in the P-type body, and it can take minutes for thermal generation to generate the necessary electrons to form the inversion layer. The MOS transistor structure shown in Fig. 5–2 solves this problem. The inversion electrons are supplied by the N^+ junctions, as shown in Fig. 5–10a. The inversion layer may be visualized as a very thin N layer (hence the term *inversion* of the surface conductivity type) as shown in Fig. 5–10b. The MOS transistor as shown in Figs. 5–2 and 5–10 is a more versatile structure for studying the MOS system than the MOS capacitor.

5.5.1 Choice of V_t and Gate Doping Type

The p-body transistor shown in Fig. 5–10 operates in an integrated circuit (IC) with V_g swinging between zero and a positive power supply voltage. To make circuit design easier, it is routine to set V_t at a small positive value, e.g., 0.4 V, so that, at $V_g = 0$, the transistor does not have an inversion layer and current does not flow between the two N^+ regions. A transistor that does not conduct current at $V_g = 0$ is called an **enhancement-type device**. This V_t value can be obtained with an N^+ gate and convenient body doping density as shown in Fig. 5–8. If the p-body device is paired with a P^+ gate,

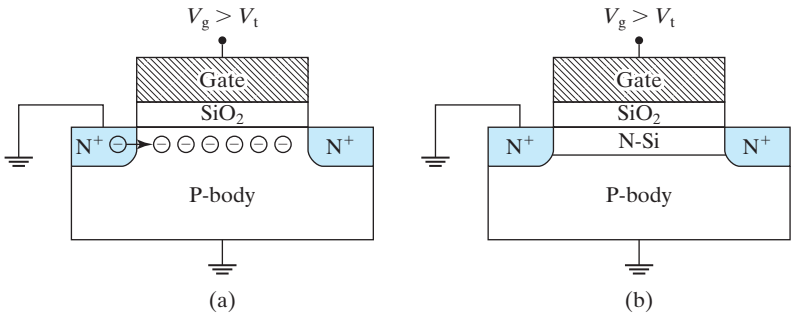

FIGURE 5–10 (a) The surface inversion behavior is best studied with a PN junction butting the MOS capacitor to supply the inversion charge. (b) The inversion layer may be thought of as a thin N-type layer.

V_t would be too large (over 1 V) and necessitate a larger power supply voltage. This would lead to larger power consumption and heat generation (see Section 6.7.3).

Similarly, an N-type body is routinely paired with a P^+ gate. In summary, P body is almost always paired with N^+ gate to achieve a small positive threshold voltage, and N body is normally paired with P^+ gate to achieve a small negative threshold voltage. The other body-gate combinations are almost never encountered.

● Review: Basic MOS Capacitor Theory ●

Let us review the concepts, nomenclatures, common approximations, and simple relationships associated with the MOS capacitor theory. We will do so using a series of figures, starting with Fig. 5–11. The surface potential, ϕ_s, is zero at V_{fb} and approximately zero in the accumulation region. As V_g increases from V_{fb} into the depletion regime, ϕ_s increases from zero toward $2\phi_B$. When ϕ_s reaches $2\phi_B$, the surface electron concentration becomes so large that the surface is considered **inverted**. The V_g at that point is called V_t, the **threshold voltage**.

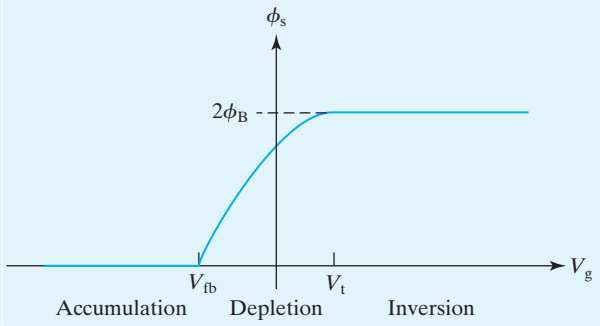

FIGURE 5–11 Surface potential saturates at $2\phi_B$ when V_g is larger than V_t.

Figure 5–12 uses W_{dep} to review the MOS capacitor. There is no depletion region when the MOS interface is in accumulation. W_{dep} in the PN junction and in the MOS capacitor is proportional to the square root of the band bending (ϕ_s in the MOS case). W_{dep} saturates at W_{dmax} when $V_g \geq V_t$, because ϕ_s saturates at $2\phi_B$.

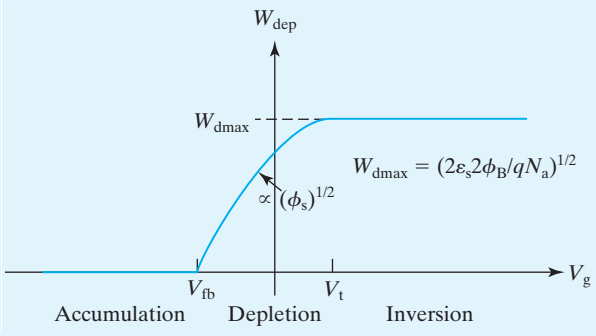

FIGURE 5–12 Depletion-region width in the body of an MOS capacitor.

Figure 5–13 reviews the three charge components in the substrate. The depletion charge Q_{dep} is constant in the inversion region because W_{dep} is a constant there. $Q_{inv} = -C_{ox}(V_g - V_t)$ appears in the inversion region. Q_{acc} shows up in the accumulation

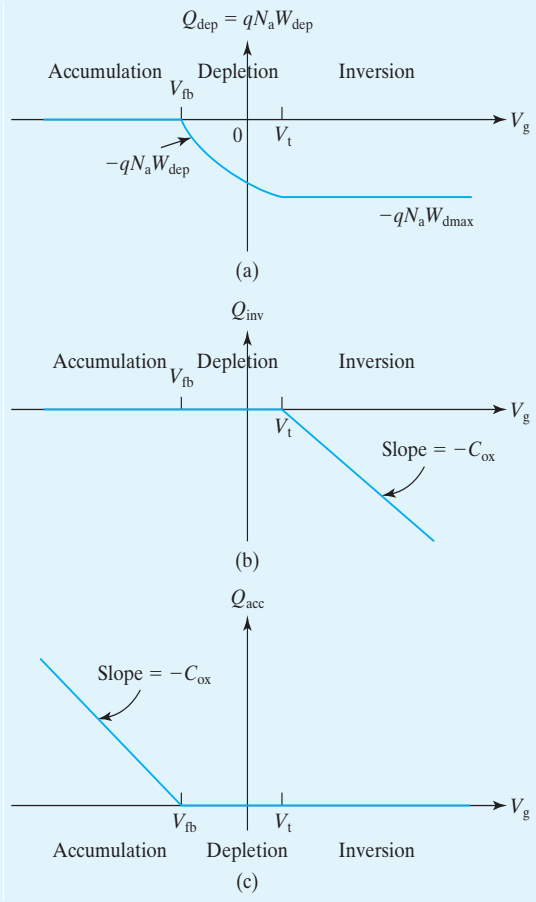

FIGURE 5–13 Components of charge (C/cm^2) in the MOS capacitor substrate: (a) depletion-layer charge; (b) inversion-layer charge; and (c) accumulation-layer charge.

region. In both (b) and (c), the slope is $-C_{ox}$. Figure 5–14 shows the total substrate charge, Q_{sub}. Q_{sub} in the accumulation region is made of accumulation charge. Q_{sub} is made of Q_{dep} in the depletion region. In the inversion region, there are two components, Q_{dep} that is a constant and Q_{inv} that is equal to $-C_{ox}(V_g - V_t)$.

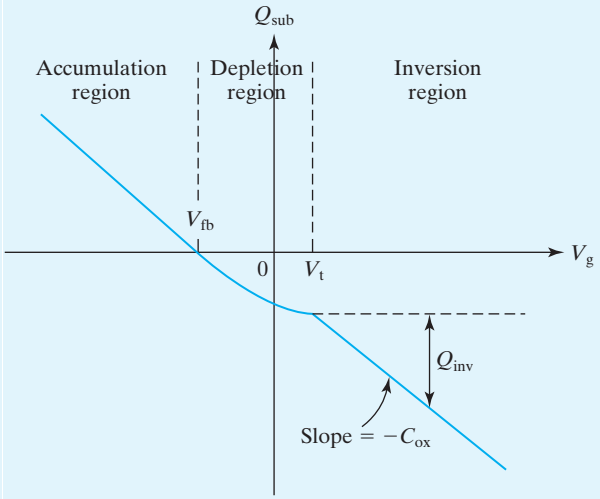

FIGURE 5–14 The total substrate charge, Q_{sub} (C/cm^2), is the sum of Q_{acc}, Q_{dep}, and Q_{inv}.

5.6 • MOS C–V CHARACTERISTICS •

The capacitance–voltage (C–V) measurement is a powerful and commonly used method of determining the gate oxide thickness, substrate doping concentration, threshold voltage, and flat-band voltage. The *C–V* curve is usually measured with a C–V meter (Fig. 5–15), which applies a DC bias voltage, V_g, and a small sinusoidal signal (1 kHz–10 MHz) to the MOS capacitor and measures the capacitive current with an AC ammeter. The capacitance is calculated from $i_{cap}/v_{ac} = \omega C$.

The capacitance in the MOS theory is always the **small-signal capacitance**

$$C \equiv \frac{dQ_g}{dV_g} = -\frac{dQ_{sub}}{dV_g} \tag{5.6.1}$$

The negative sign in Eq. (5.6.1) arises from the fact that V_g is taken at the top capacitor plate but Q_{sub} is taken at the bottom capacitor plate (the body). Q_{sub} is given in Fig. 5–14 and its derivative is shown in Fig. 5–16.

In the accumulation region, the MOS capacitor is just a simple capacitor with capacitance C_{ox} as shown in Fig. 5–17a. Figure 5–17b shows that in the depletion region, the MOS capacitor consists of two capacitors in series: the oxide capacitor, C_{ox}, and the depletion-layer capacitor, C_{dep}. Under the AC small-signal voltage, W_{dep} expands and contracts slightly at the AC frequency. Therefore, the AC charge appears at the bottom of the depletion layer as shown in Fig. 5–17b.

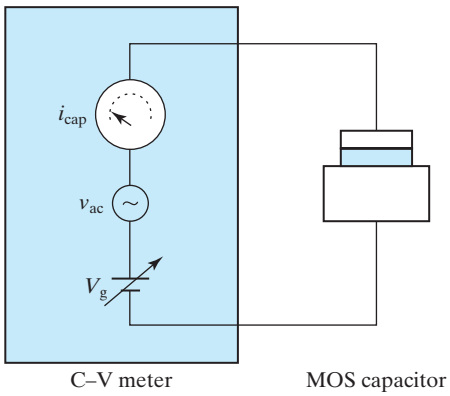

FIGURE 5–15 Setup for the C–V measurement.

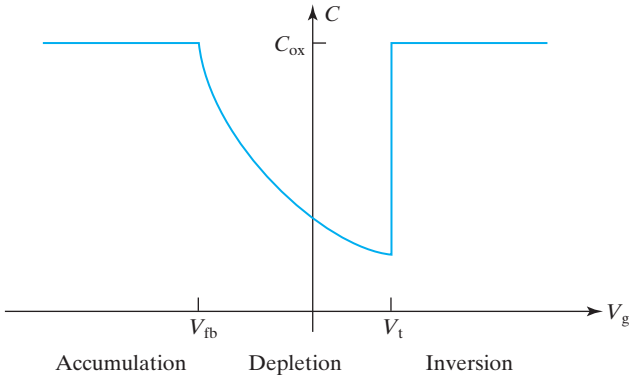

FIGURE 5–16 The quasi-static MOS C–V characteristics.

$$C_{dep} = \frac{\varepsilon_s}{W_{dep}} \tag{5.6.2}$$

$$\frac{1}{C} = \frac{1}{C_{ox}} + \frac{1}{C_{dep}} \tag{5.6.3}$$

$$\frac{1}{C} = \sqrt{\frac{1}{C_{ox}^2} + \frac{2(V_g - V_{fb})}{qN_a\varepsilon_s}} \tag{5.6.4}$$

To derive Eq. (5.6.4), one needs to solve Eq. (5.3.3) for W_{dep} as a function of V_g. The derivation is left as an exercise for the reader in the problems section at the end of the chapter. As V_g increases beyond V_{fb}, W_{dep} expands, and therefore C decreases as shown in Fig. 5–16.

Figure 5–17c shows that an inversion layer exists at the Si–SiO_2 interface. In response to the AC signal, Q_{inv} increases and decreases at the AC frequency. The inversion layer plays the role of the bottom electrode of the capacitor. Therefore, C reverts to C_{ox} in the inversion region as shown in Fig. 5–16. This C–V curve is called

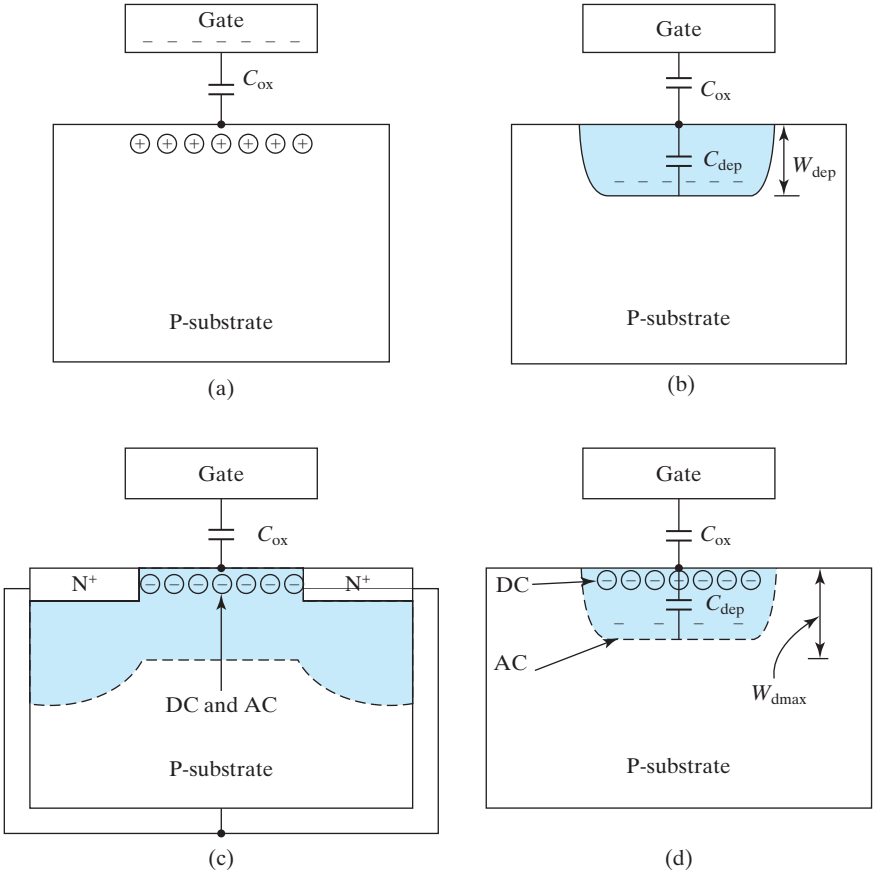

FIGURE 5–17 Illustration of the MOS capacitor in all bias regions with the depletion-layers shaded. (a) Accumulation region; (b) depletion region; (c) inversion region with efficient supply of inversion electrons from the N region corresponding to the transistor *C–V* or the quasi-static *C–V*; and (d) inversion region with no supply of inversion electrons (or weak supply by thermal generation) corresponding to the high-frequency capacitor *C–V* case.

the **quasi-static C–V** because Q_{inv} can respond to the AC signal as if the frequency were infinitely low (static case). That would require a ready source of electrons, which can be provided by the N region shown in Fig. 5–17c. PN junctions are always present in an MOS transistor. Therefore, the **MOS transistor C–V** characteristics at all frequencies follow the curve in Fig. 5–16, which is repeated as the upper curve in Fig. 5–18.

What if, as in Fig. 5–17d, the PN junctions are not present? The P-type substrate is an inefficient supplier of electrons. It produces electrons through thermal generation at a very slow rate (for the same reason the diode reverse leakage current is small.) Q_{inv} cannot respond to the AC signal and remains constant at its DC value. Instead, the AC signal causes ϕ_s to oscillate around $2\phi_B$

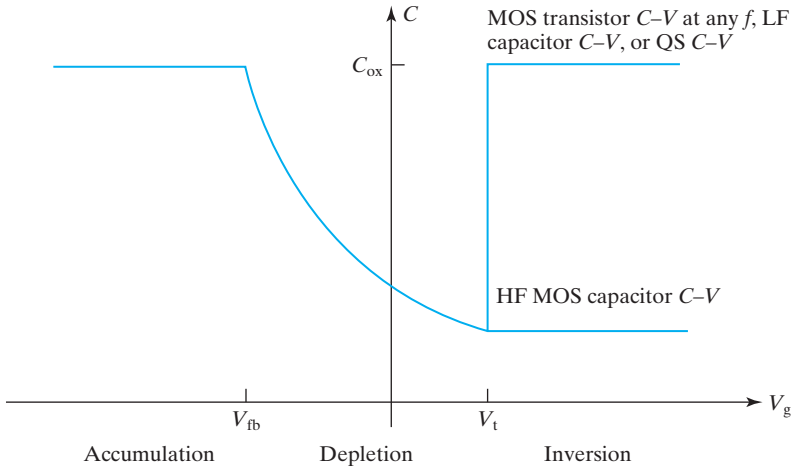

FIGURE 5–18 Two possible MOS C–V characteristics. The difference in the inversion region is explained in Fig. 5–17c and d.

and causes W_{dep} to expand and contract slightly around W_{dmax}. This change of W_{dep} can respond at very high frequencies because it only involves the movement of the abundant majority carriers. Consequently, the AC charge exists at the bottom of the depletion region. The result is a saturation of C at V_t as illustrated by the lower curve in Fig. 5–18. This curve is known as the capacitor C–V or the **high-frequency MOS capacitor *C–V*** (HF *C–V*). The name connotes that, in principle, at a sufficiently low frequency, even the MOS capacitor's C–V would follow the upper curve in Fig. 5–18. Following that reasoning, the upper curve is also known as the **low-frequency *C–V*** (LF *C–V*)**.** In reality, even at a low frequency such as 1 kHz, the C–V of modern high-quality MOS capacitors does not follow the LF *C–V* curve. At yet lower frequencies, the C–V meter is ineffective (the capacitative current is too low) for studying the MOS capacitor. The term *low-frequency C–V* has a historical significance and is still used, but it no longer has a practical significance.

• Measuring the Quasi-Static C–V Using an MOS Capacitor •

There *is* a practical way to obtain the "low frequency" or quasi-static *C–V* (upper branch of Fig. 5–18) using an MOS capacitor without the PN junction. It involves applying a very slow linear-ramp voltage (<0.1V/s) to the gate and measuring I_g with a very sensitive DC ammeter during the ramp. C is calculated from $I_g = C \cdot dV_g/dt$. This technique provides sufficient time for Q_{inv} to respond to the slowly changing V_g. Plotting $I_g/(dV_g/dt)$ vs. V_g produces the QS *C–V* curve shown in Fig. 5–18. This technique becomes impracticable if the gate dielectric has too large a leakage current.

EXAMPLE 5–1 C–V of MOS Capacitor and Transistor

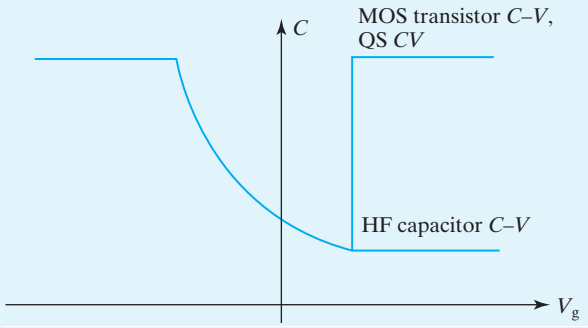

FIGURE 5–19 *C–V* curves of MOS capacitor and transistor.

For each of the following cases, does the QS *C–V* or the HF capacitor *C–V* apply?

(1) MOS transistor, 10 kHz. (Answer: QS *C–V*).
(2) MOS transistor, 100 MHz. (Answer: QS *C–V*).
(3) MOS capacitor, 100 MHz. (Answer: HF capacitor *C–V*).
(4) MOS capacitor, 10 kHz. (Answer: HF capacitor *C–V*).
(5) MOS capacitor, slow V_g ramp. (Answer: QS *C–V*).
(6) MOS transistor, slow V_g ramp. (Answer: QS *C–V*).

5.7 • OXIDE CHARGE—A MODIFICATION TO V_{fb} AND V_t[4] •

The basic MOS theory ignores the possible presence of electric charge in the gate dielectric. Assuming surface charge, Q_{ox} (C/cm^2), exists at the SiO_2–Si interface, the band diagram at the flat-band condition would be modified from Fig. 5–20a to 5–20b.

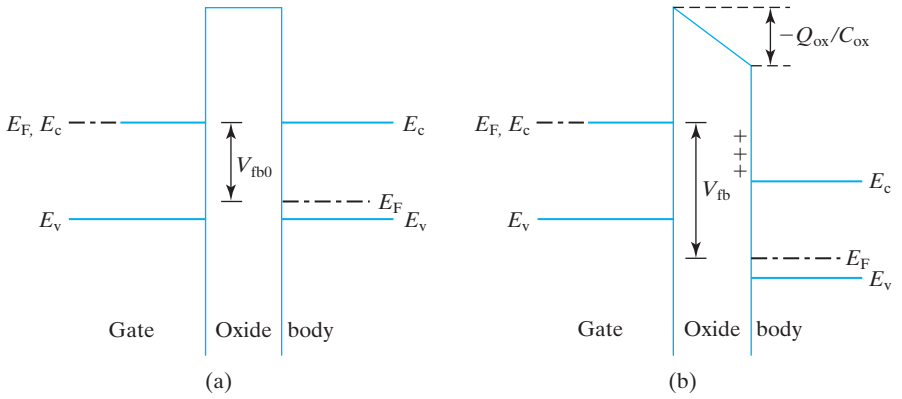

FIGURE 5–20 Flat-band condition (no band bending at body surface) (a) without any oxide charge; (b) with Q_{ox} at the oxide–substrate interface.

[4] This section may be omitted in an accelerated course.

The flat-band voltage in Fig. 5–20a is $\psi_g - \psi_s$ (Section 5.1). In Fig. 5–20b, the oxide charge (assumed to be located at the oxide–substrate interface for simplicity) induces an electric field in the oxide and an oxide voltage, $-Q_{ox}/C_{ox}$. Clearly, V_{fb} in part b is different from the V_{fb0} in part a. Specifically,

$$V_{fb} = V_{fb0} - Q_{ox}/C_{ox} = \psi_g - \psi_s - Q_{ox}/C_{ox} \tag{5.7.1}$$

Because Q_{ox} changes V_{fb}, it also changes V_t through Eq. (5.4.3).

There are several types of **oxide charge**. Positive **fixed oxide charge** is attributed to silicon ions present at the Si–SiO_2 interface. **Mobile oxide charge** is believed to be mostly sodium ions. Mobile ions can be detected by observing V_{fb} and V_t shift under a gate bias at an elevated temperature (e.g., at 200 °C) due to the movement of the ions in the oxide. **Sodium contamination** must be eliminated from the water, chemicals, and containers used in an MOS fabrication line in order to prevent instabilities in V_{fb} and V_t. In addition, significant **interface traps** or **interface states** may be present and they can trap and release electrons and generate noise (see Section 6.15.3) and degrade the subthreshold current of MOSFET (see Section 7.2).

● Reliability ●

More interface states and fixed oxide charge appear after the oxide is subjected to high electric field for some time due to the breaking or rearrangement of chemical bonds. This raises a reliability concern because the threshold voltage and transistor current would change with usage and can potentially cause sensitive circuits to fail. Engineers ensure device reliability by controlling the stress field and improving the MOS interface quality and verifying or projecting the reliability with careful long-term testing.

EXAMPLE 5–2 Interpret the measured V_{fb} dependence on oxide thickness in Fig. 5–21 using Eq. (5.7.1). It is known that the gate electrode is N^+ poly-Si. What can you tell about the capacitors?

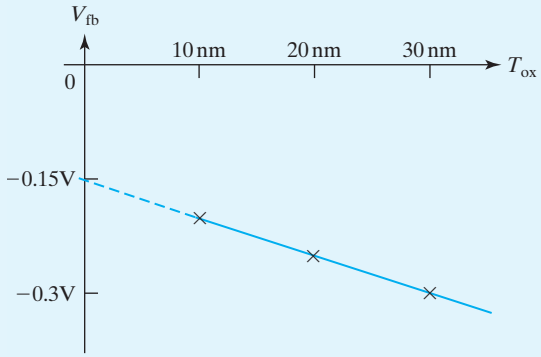

FIGURE 5–21 Measured V_{fb} of three capacitors with different oxide thicknesses.

SOLUTION:

$$V_{fb} = \psi_g - \psi_s - Q_{ox}T_{ox}/\varepsilon_{ox} \tag{5.7.1}$$

Equation (5.7.1) suggests that V_{fb} at $T_{ox} = 0$ is $\psi_g - \psi_s$. Therefore, $\psi_g - \psi_s = -0.15$ V. This is illustrated in Fig. 5–22.

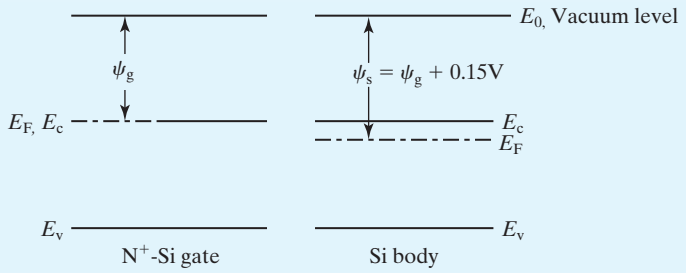

FIGURE 5–22 The relationship between ψ_g and ψ_s.

Because E_F is 0.15 V below E_c, we conclude that the substrate is N-type with

$$N_d = n = N_c e^{-0.15\,eV/kT} \approx 10^{17}\,cm^{-3}$$

Further, Eq. (5.7.1) suggests that

$$Q_{ox} = -\varepsilon_{ox} \times \text{slope of line in Fig. 5–21}$$

$$= -\varepsilon_{ox} \times \frac{-0.15\ V}{30\ nm} = \frac{3.9 \times 8.85 \times 10^{-14} \times 0.15\ V}{300 \times 10^{-8}} = 1.7 \times 10^{-8}\ C/cm^2$$

This corresponds to 1.7×10^{-8} cm$^2 \div q = 9 \times 10^{10}$ cm^2 of positive charge at the interface. A high-quality MOS interface has about 10^{10} cm^2 of charge. Both numbers are small fractions of the number of silicon atoms on a (100) crystal plane, 7×10^{14} cm^{-2}. In this sense, the SiO_2–Si interface is remarkably well-behaved and charge-free.

5.8 • POLY-SI GATE DEPLETION—EFFECTIVE INCREASE IN T_{OX} •

Consider an MOS capacitor with P^+ poly-Si gate and N body. The capacitor is biased into surface inversion. Figure 5–23a shows that the continuity of electric flux requires that the band bends in the gate. This indicates the presence of a thin depletion layer in the gate. Depending on the gate doping concentration and the oxide field, the ***poly-Si gate depletion*** layer thickness, W_{dpoly}, may be 1–2 nm. According to Gauss's Law,

$$W_{dpoly} = \varepsilon_{ox}\mathscr{E}_{ox}/qN_{poly} \tag{5.8.1}$$

Because a depletion layer is present in the gate, one may say that a poly-silicon-gate capacitor is added in series with the oxide capacitor as shown in Fig. 5–23b. The MOS capacitance in the inversion region becomes

$$C = \left(\frac{1}{C_{ox}} + \frac{1}{C_{poly}}\right)^{-1} = \left(\frac{T_{ox}}{\varepsilon_{ox}} + \frac{W_{dpoly}}{\varepsilon_s}\right)^{-1} = \frac{\varepsilon_{ox}}{T_{ox} + W_{dpoly}/3} \tag{5.8.2}$$

This **poly-depletion effect** effectively increases T_{ox} by $W_{dpoly}\varepsilon_{ox}/\varepsilon_s$ or $W_{dpoly}/3$, and can have a significant impact on the C–V curve if T_{ox} is thin. The gate capacitance drops as the capacitor is biased deeper into the inversion region due to increasing poly-depletion as shown in Fig. 5–26. The poly-depletion effect is

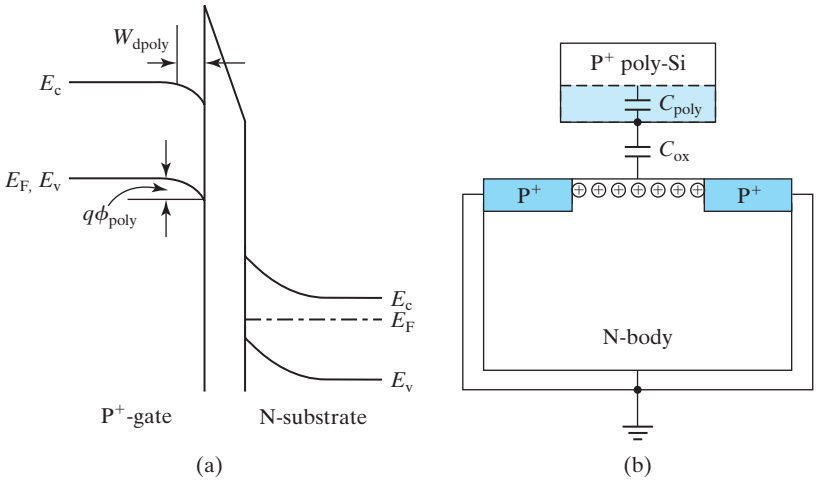

FIGURE 5–23 Poly-gate depletion effect illustrated with (a) the band diagram and (b) series capacitors representation. An N^+ poly-Si gate can also be depleted.

undesirable because a reduced C means reduced Q_{inv}, and reduced transistor current. The solution is to dope the poly-Si heavily. Unfortunately, very heavy doping may cause **dopant penetration** from the gate through the oxide into the substrate. **Poly-SiGe** gate can be doped to a higher concentration, thus improving gate depletion [1]. Poly-gate depletion is eliminated in advanced MOSFET technology by substitution of the poly-gate with a metal gate (see Section 7.4).

The effect of poly-gate depletion on Q_{inv} may be modeled in another way:

$$Q_{inv} = -C_{ox}(V_g - \phi_{poly} - V_t) \tag{5.8.3}$$

Poly-gate depletion effectively reduces V_g by ϕ_{poly}. Even 0.1 V ϕ_{poly} would be highly undesirable when the power-supply voltage (the maximum V_g) is only around 1 V.

EXAMPLE 5–3 Poly-Si Gate Depletion

Assume that V_{ox}, the voltage across a 2 nm thin oxide is –1 V. The P^+ poly-gate doping is $N_{poly} = 8 \times 10^{19}$ cm^3 and substrate N_d is 10^{17}cm^3. Estimate (a) W_{dpoly}, (b) ϕ_{poly}, and (c) V_g.

SOLUTION:

a. Using Eq. (5.8.1),

$$W_{dpoly} = \varepsilon_{ox}\mathscr{E}_{ox}/qN_{poly} = \varepsilon_{ox}V_{ox}/T_{ox}qN_{poly}$$

$$= \frac{3.9 \times 8.85 \times 10^{-14}(\text{F/cm}) \cdot 1\text{V}}{2 \times 10^{-7}\text{cm} \cdot 1.6 \times 10^{-19}\text{C} \cdot 8 \times 10^{19}\text{cm}^{-3}}$$

$$= \frac{34.5 \times 10^{-14}\text{cm}}{256 \times 10^{-8}} = 0.13 \times 10^{-6}\text{cm} = 1.3\,\text{nm}$$

b. W_{dpoly} is related to ϕ_{poly} by the depletion-region model

$$W_{dpoly} = \sqrt{\frac{2\varepsilon_s \phi_{poly}}{qN_{poly}}}$$

$$\phi_{poly} = qN_{poly}W_{dpoly}{}^2/2\varepsilon_s$$

$$= \frac{1.6\times10^{-19}\text{C}\cdot 8\times10^{19}\text{cm}^{-3}\cdot(1.3\times10^{-7}\text{cm})^2}{2\times12\times8.85\times10^{-14}\text{F/cm}}$$

$$= \frac{2.3\times10^{-13}\text{V}}{2.1\times10^{-12}} = 0.11\text{ V}$$

c. Equation (5.2.2) with a ϕ_{poly} term added is

$$V_g = V_{fb} + \phi_{st} + V_{ox} + \phi_{poly}$$

$$V_{fb} = \psi_g - \psi_s = \frac{E_g}{q} - \frac{kT}{q}\ln\frac{N_c}{N_d} = 1.1 - 0.15\text{ V} = 0.95\text{ V}$$

$$V_g = 0.95 - 0.8 - 1 - 0.11\text{ V} = -0.96\text{ V}$$

Using Eq. (5.4.5), $\phi_{st} = -2\phi_B = -2\frac{kT}{q}\ln\frac{N_d}{n_i} = -0.8$

Draw an energy band diagram to confirm the signs of terms in the last equation. The loss of 0.11 V to poly-depletion is a large loss relative to the 0.96 V applied voltage.

5.9 • INVERSION AND ACCUMULATION CHARGE-LAYER THICKNESSES AND QUANTUM MECHANICAL EFFECT •

So far, we have implicitly assumed that the inversion charge is a sheet charge at the Si–SiO_2 interface (i.e., the inversion layer is infinitely thin). In reality, the inversion-charge profile is determined by the solution of the Schrödinger equation and Poisson's equation [2]. For this reason, the present topic is often referred to as the **quantum mechanical effect** in an MOS device. An example of the charge profile is shown in Fig. 5–24. The average location or centroid of the inversion charge below the Si–SiO_2 interface is called the **inversion-layer thickness**, $\boldsymbol{T_{inv}}$. Figure 5–25 shows T_{inv} as a function of V_g. When V_g is large, T_{inv} is around 1.5 nm. When V_g is low, T_{inv} can be 3 nm. It is shown in Eq. (6.3.6) that

$$\text{average field in the inversion layer} = \frac{V_g + V_t}{6T_{ox}} \tag{5.9.1}$$

It is reasonable that T_{inv} is a function of the average field, and therefore a function of $(V_g + V_t)/T_{ox}$ as shown in Fig. 5–25. The electron inversion layer is thinner than the hole inversion layer because the electron effective mass is smaller. It is valid to think that the bottom electrode of the MOS capacitor is not exactly at the Si–SiO_2 interface

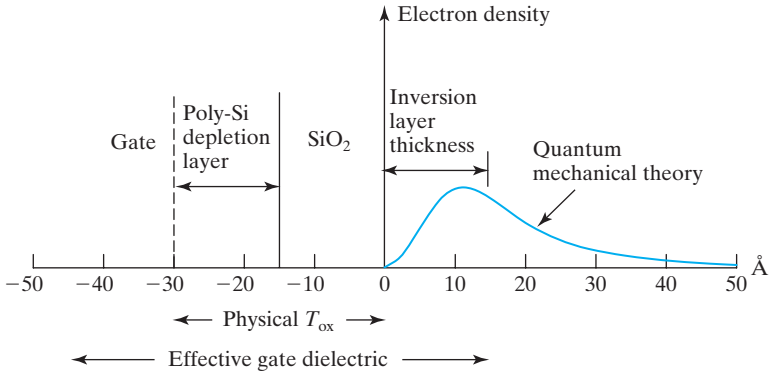

FIGURE 5–24 Average location of the inversion-layer electrons is about 15 Å below the Si–SiO_2 interface. Poly-Si gate depletion is also shown.

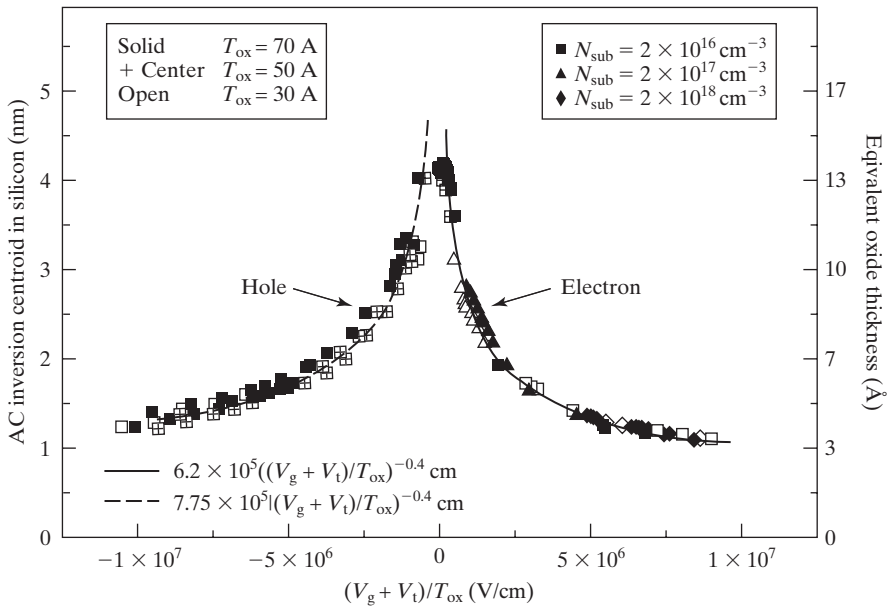

FIGURE 5–25 Average inversion-layer thickness (centroid) for electrons (in P body) and holes (in N body). (From [3]. © 1999 IEEE.)

but rather effectively located below the interface by T_{inv}. In other words, T_{ox} is effectively increased by $T_{inv}/3$, where 3 is the ratio of $\varepsilon_s/\varepsilon_{ox}$. The accumulation layer has a similar thickness. The effect on the C–V characteristics (shown in Fig. 5–26) is to depress the *C–V* curve at the onset of inversion and accumulation. Figure 5–27 explains the transition of the *C–V* curve in Fig. 5–26 from the depletion to the inversion region. Figure 5–27a is the general case. In the depletion region, C_{inv} is negligible (there is no inversion charge) and C_{poly} can be neglected because $W_{dpoly} << W_{dep}$. Therefore, Fig. 5–27 reduces to the basic series combination of C_{ox} and C_{dep} of Fig. 5–27b. As V_g increases toward V_t, C_{inv} increases as the inversion charge begins to appear, and the total capacitance rises above the basic *C–V* as shown in Fig. 5–27c and

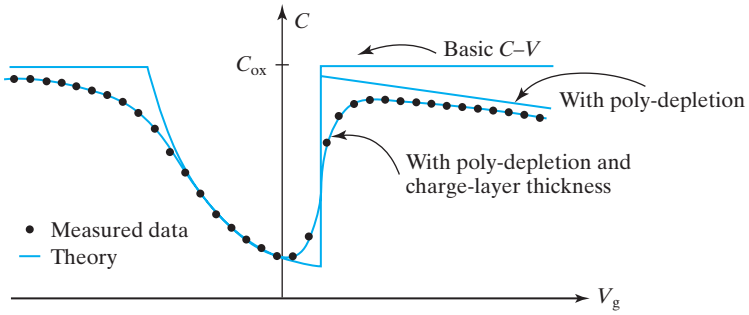

FIGURE 5–26 The effects of poly-depletion and charge-layer thickness on the *C–V* curve of an N^+ poly-gate, P-substrate device.

Fig. 5–26. The capacitance rises smoothly toward C_{ox} because the inversion charge is not located exactly at the silicon–oxide interface, but at some depth that varies with V_g as shown in Fig. 5–25. At larger V_g, C_{poly} cannot be assumed to be infinity (W_{dpoly} increases), and C drops in Fig. 5–26.

T_{inv} and W_{dpoly} used to be negligible when T_{ox} was large (>10 nm). For thinner oxides, they are not. Because it is difficult to separate T_{ox} from T_{inv} and W_{dpoly} by measurement, an **electrical oxide thickness**, $\boldsymbol{T_{oxe}}$, is often used to characterize the total effective oxide thickness. T_{oxe} is deduced from the inversion-region capacitance measured at $V_g = V_{dd}$. One may think of T_{oxe} as an **effective oxide thickness**, corresponding to an **effective gate capacitance**, C_{oxe}. T_{oxe} is the sum of three thicknesses,

$$T_{oxe} = T_{ox} + W_{dpoly}/3 + T_{inv}/3 \tag{5.9.2}$$

where 3 is the ratio of $\varepsilon_s/\varepsilon_{ox}$, which translates W_{dpoly} and T_{inv} into equivalent oxide thicknesses. The total inversion charge per area, Q_{inv}, is

$$\boxed{\begin{aligned} Q_{inv} &= -C_{oxe}(V_g - V_t) \\ &= \frac{\varepsilon_{ox}}{T_{oxe}}(V_g - V_t) \end{aligned}} \tag{5.9.3}$$

Typically, T_{oxe} is larger than T_{ox} by 6–10 Å.

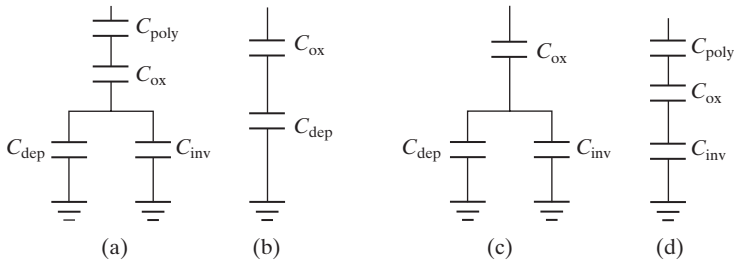

FIGURE 5–27 Equivalent circuit for understanding the *C–V* curve in the depletion region and the inversion region. (a) General case for both depletion and inversion regions; (b) in the depletion regions; (c) $V_g \approx V_t$; and (d) strong inversion.

In addition, there is another quantum effect that increases the threshold voltage [4]. At high substrate doping concentration, the high electric field in the substrate at the oxide interface in Fig. 5–7 causes the energy levels to be quantized and effectively increases E_g and decreases n_i in Eq. (5.4.1). This requires the band to bend down more before reaching threshold, i.e., causes ϕ_{st} in Eq. (5.4.2) to increase. The net effect is that the threshold voltage is increased by 100mV or so depending on the doping concentration due to this **quantum effect on threshold voltage**.

5.10 • CCD IMAGER AND CMOS IMAGER •

An **imager** is a sensing device that converts an optical image into an electronic signal. CCD imager and CMOS imager are used in digital cameras and camcorders. CCD imagers have higher performance but are more expensive. CMOS imagers are newer and less expensive. They are presented in the next two sub-sections.

5.10.1 CCD Imager

CCD stands for **charge-coupled device** [5]. The heart of a CCD imager is a large number of MOS capacitors densely packed in a two-dimensional array.

Let us first consider how a single MOS capacitor reacts to light. Figure 5–28a shows an MOS capacitor biased into **deep-depletion**. A voltage, $V_g > V_t$, has been suddenly applied to the gate. Because thermal generation is a slow process, there

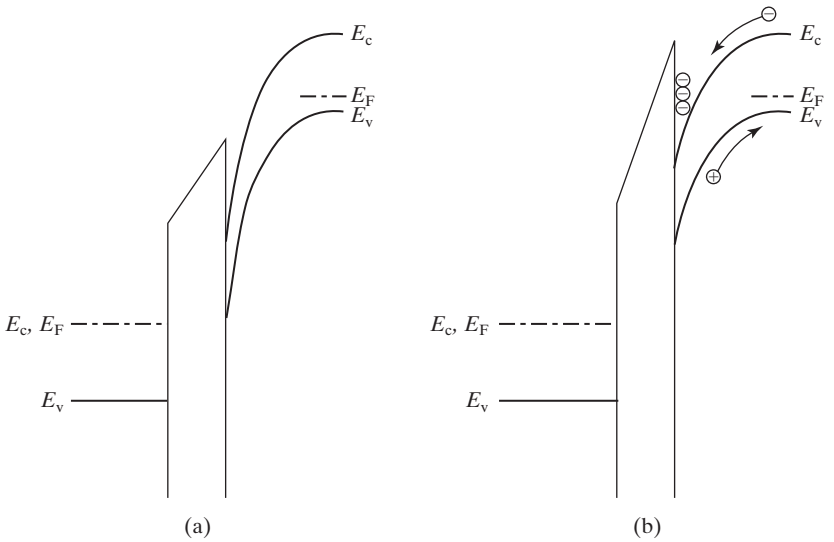

FIGURE 5–28 Deep depletion. (a) Immediately after a gate voltage $V_g >$, V_t is applied, there are no electrons at the surface. (b) After exposure to light, photo-generated electrons have been collected at the surface. The number of electrons is proportional to the light intensity.

are no electrons (no inversion layer) at the surface during at least the first fraction of a second. As a result, the band bends beyond $2\phi_B$ and the depletion region extends beyond W_{dmax}. This condition is called deep depletion. If light shines on the MOS capacitor in this condition for ten milliseconds, some photo-generated electrons will be collected at the interface as shown in Fig. 5–28b. The photo-generated holes flow into the substrate and are removed through the substrate contact. The number of electrons collected is proportional to the light intensity. This is the first function of a CCD array—to convert an image (two-dimensional pattern of light intensity) into packets of electrons stored in a two-dimensional array of MOS capacitors.

● Deep-Depletion C–V ●

If an MOS capacitor is biased into deep depletion by rapidly sweeping the gate bias, W_{dep} may exceed W_{dmax}. As a result, the capacitance continues to fall even at $V_g > V_t$ as shown in Fig. 5–29. Deep-depletion C–V again illustrates the impossibility of establishing the inversion layer rapidly in an MOS capacitor (without a PN junction supplying the inversion charge).

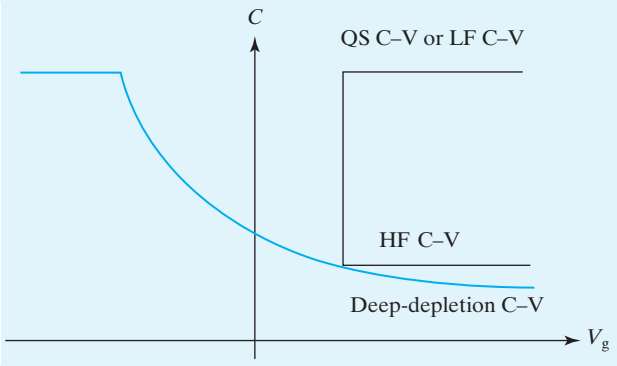

FIGURE 5–29 Deep-depletion C–V.

The second function of a CCD array is to transfer the collected charge packets to the edge of the array, where they can be read by a charge sensing circuit in a serial manner. To illustrate this charge transfer function, let us examine the one-dimensional array in Fig. 5–30, representing a small portion of a single row in the two-dimensional array. Every three MOS capacitors or elements constitute one sensor pixel. In Fig. 5–30a, exposure to a lens-projected image has produced some electrons in the element on the right, even more in the element on the left and yet more in the middle element in proportion to the image light intensity around those three locations. Electrons are collected only under these three elements, not the ones flanking them, because these three are biased to deeper band bendings (more positive ϕ_s) than their neighbor elements and any electrons that might show up in the neighbors would flow to these three more positive locations. Under the bias condition of Fig. 5–30b, V_2 creates the deepest depletion. After the gate biases are switched from (a) to (b), the charge packets will move to the elements connected to V_2 (i.e., shifted to the right by one element). The choice of $V_1 > V_3$ ensures that no

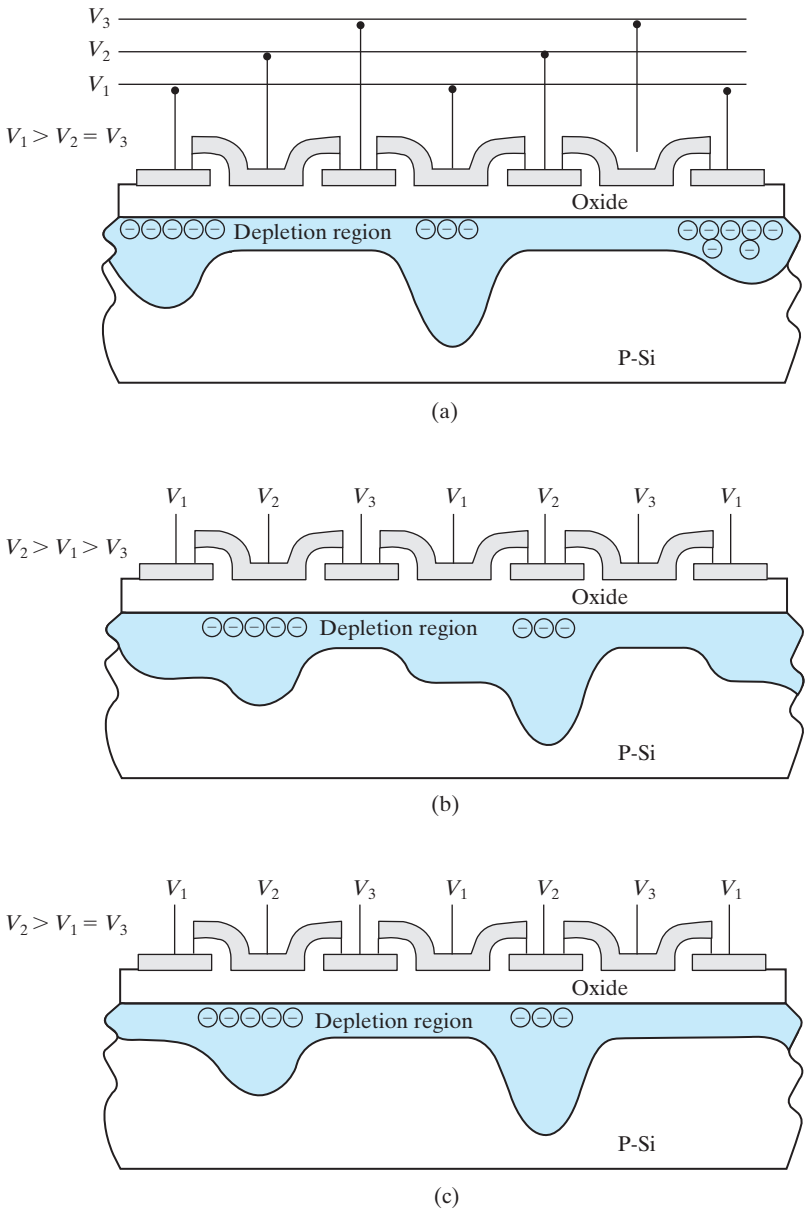

FIGURE 5–30 How CCD shifts the charge packets. The array is biased in the sequence (a), (b), (c), (a), (b), (c), (a) ... . The drawing in (c) is identical to (a) but with all the charge packets shifted to the right by one capacitor element.

electrons are transferred to the left. Finally, in step (c), V_1 is reduced to the same value as V_3, thus making (c) identical to (a), except for the shift of the electron packets to the right, setting the stage for the next transfer operation. In this manner, the electron packets are shifted to the right element by element. Waiting at the right edge of the array is a charge-sensing circuit that generates a serial voltage signal that faithfully represents the image light pattern. In summary, a CCD imager first

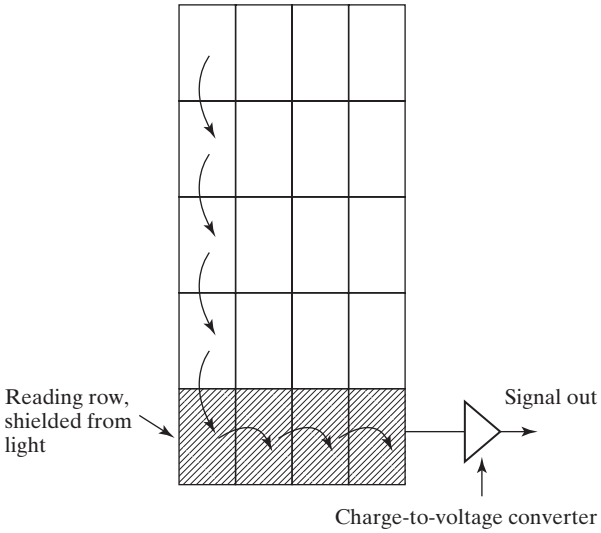

FIGURE 5–31 Architecture of a two-dimensional CCD imager. The arrows show the path of the charge-packet movement.

converts light patterns into patterns of electron packets and then transfers the charge packets one element at a time to the edge of the array, where they are converted into a serial electrical signal by a charge-sensing circuit. For example, the three charge packets in Fig. 5–30 would generate a small signal pulse, followed by a large pulse, and then a medium pulse.

Figure 5–31 depicts a two-dimensional CCD imager containing four rows and four columns of 16 MOS capacitors plus a reading row at the bottom. The reading row is shielded from the light by a metal film. The two-dimensional charge packets are read row by row. First, the charge packets in the 16 elements are shifted downward by one row. This action transfers the charge packets in the lowest sensing row (the fourth row from the top) into the reading row. Next, the charge packets in the reading row only are shifted to the right. To the right side of the row is a circuit that converts each arriving charge packet into a voltage pulse. After the packets of the fourth row have been read in this way, the remaining three rows of charge packets are shifted downward by one row again. Now the reading row begins to shift the new row of charge packets to the converter circuit. During the shifting-and-reading operation, the CCD array is blocked from light with a mechanical shutter. Otherwise, the image would be smeared. For example, the charge packets in the top row would be exposed to the light patterns of the other rows during the shifting and reading.

5.10.2 CMOS Imager

CMOS imagers do not shift the charge packets from row to row. They do not need mechanical shutters, use less power, and are cheaper than CCD imagers. For these reasons, CMOS imagers made mobile phone cameras practical and are widely used in low-cost digital cameras. In a CMOS imager, the charge collected in an array element is converted into voltage by a circuit integrated in that array element as

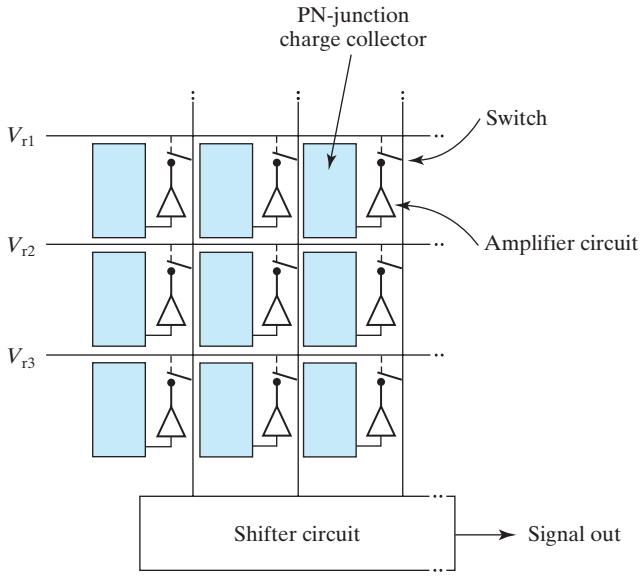

FIGURE 5–32 Architecture of a CMOS imager. Each array element has its own charge-to-voltage converter represented by the triangle. Actual imagers may support hundreds to over a thousand rows and columns of pixels.

shown in Fig. 5–32. An open-circuited N^+P junction collects the light-generated charge. The P substrate is grounded. Electrons generated by light near the PN junction diffuse to the junction and get collected and stored in the thin N^+ region. Since the PN junction is a capacitor, the stored electrons change the capacitor voltage, i.e., the N^+-region voltage. This voltage is amplified in the pixel as shown in Fig. 5–32.

Each pixel also contains a switch made of an MOS transistor and controlled by the voltages V_{r1}, V_{r2}, or V_{r3} that is carried by long horizontal metal lines. In order to read the top row of pixels, V_{r1} is raised to turn on (close) all the switches in the top row. This brings the signals from all the top-row pixels to the shifter circuit below by vertical-running metal lines.

CMOS imagers became attractive only after transistor size reduction made the circuitry in each array element, employing half a dozen or more transistors, small in comparison with the element area. CMOS imagers are so named because their circuitry and the N^+P junctions are fabricated with CMOS circuit (see Section 6.2) technology. CMOS IC technology is the mainstream manufacturing technology and its high volume has driven the wafer cost of CMOS imagers below that of CCD imagers. Because they share the same CMOS technology, CMOS imagers can be integrated with signal processing and control circuitries to further reduce system costs. A CMOS imager's image uniformity and contrast ratio are not as good as those of a CCD. The size constraint of the sensing circuits forces the CMOS imager to use very simple circuits and it is difficult to avoid variations among the very large number of sensing circuits. In contrast, a CCD imager employs a small number of sophisticated sensing circuits.

• Color Imagers •

A color imager must produce three separate signals for the red, green, and blue light in the image. A color pixel usually contains four sensor array elements. The upper-left element senses red light. The upper-right senses green and the lower-right senses blue. The lower-left element senses green again because the human eye is more sensitive to the green light than red and blue. The color designation is accomplished by coating the elements with red, green, or blue filter films. These films containing color dyes may be deposited by a spin-on process and patterned with photolithography similar to photoresists (Section 3.3).

5.11 • CHAPTER SUMMARY •

The three regions **(accumulation, depletion, and inversion)** and the two transition points **(flat-band and threshold)** are reviewed in Fig. 5–33 for the two prevalent MOS device types. Upward arrows indicate negative V_g and downward arrows, positive V_g. Please review this figure carefully.

The flat-band voltage is

$$V_{fb} = \psi_g - \psi_s - Q_{ox}/C_{ox} \tag{5.7.1}$$

ψ_g and ψ_s are the gate and substrate work functions. Q_{ox} is a sheet charge that may be present at the SiO_2–Si interface. The gate voltage in excess of V_{fb} is divided between the substrate and the oxide and the poly-gate depletion layer.

$$V_g = V_{fb} + \phi_s + V_{ox} + \phi_{poly} \tag{5.2.2 \& Sec. 5.8}$$

$$= V_{fb} + \phi_s - Q_{sub}/C_{ox} + \phi_{poly} \tag{5.2.6}$$

ϕ_s is the surface potential, or the substrate band bending. V_{ox} is the oxide voltage. Q_{sub} (C/cm^2) is all the accumulation, inversion, and depletion-layer charge. At the **threshold** of inversion, ϕ_s is

$$\phi_{st} = \pm 2\phi_B \tag{5.4.2 \& 5.4.5}$$

$$\phi_B = \frac{kT}{q} \ln \frac{N_{sub}}{n_i} \tag{5.4.2 \& 5.4.6}$$

$$V_t = V_{fb} + \phi_{st} \pm \frac{\sqrt{qN_{sub}2\varepsilon_s|\phi_{st}|}}{C_{ox}} \tag{5.11.5 \& 5.4.4}$$

In the last three equations, the positive signs are for a P substrate (band bending downward) and the negative signs are for an N substrate (band bending upward).

There are two types of *C–V* curves as shown in Fig. 5–34. The quasi-static (QS) *C–V* curve, also known as the LF *C–V*, is applicable when the inversion charge can rapidly follow the change in V_g. It is the MOS transistor C–V at all frequencies because the short-circuited PN junction is a source of Q_{inv}. The lower *C–V* curve, the capacitor (HF) *C–V*, is applicable when Q_{inv} cannot follow the change in AC V_g. A third C–V curve, the deep-depletion C–V (Fig. 5–29), applies when Q_{inv} cannot even follow the rapid change in the bias V_g.

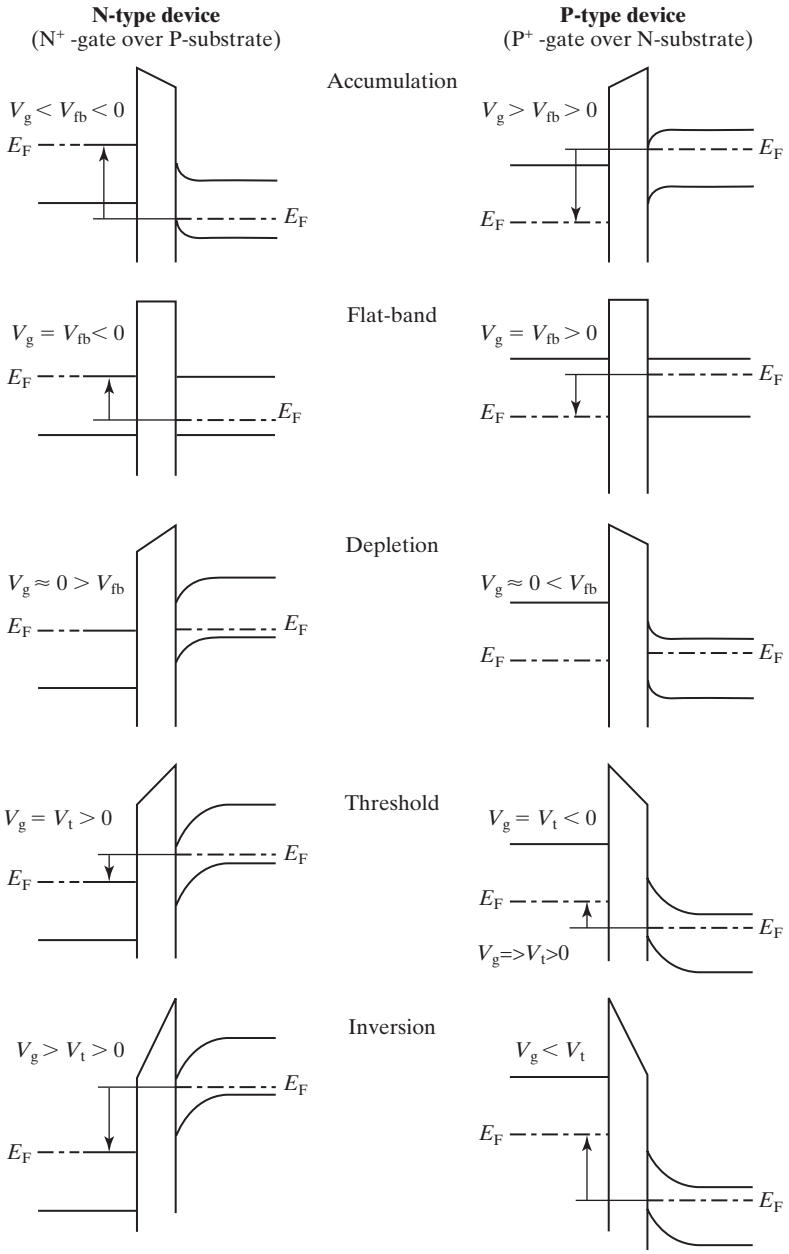

FIGURE 5–33 Energy band diagrams of the two dominant types of MOS capacitors. An N-type device is so named because it has N-type inversion charge that increases with a more positive V_g, and a P-type device has P-type inversion charge increasing with a more negative V_g.

The finite thickness of the inversion and accumulation layers, T_{inv} and T_{acc}, effectively increases T_{ox} by $T_{inv}/3$ and $T_{acc}/3$. The electrical oxide thicknesses is

$$T_{oxe} = T_{ox} + W_{dpoly}/3 + T_{ch}/3 \tag{5.9.2}$$

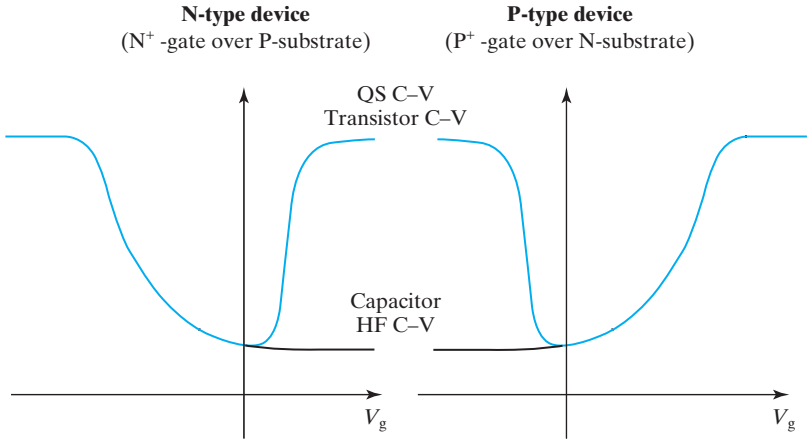

FIGURE 5–34 N-type and P-type MOS capacitors.

The number 3 is the ratio of silicon permittivity (11.9) to SiO_2 permittivity (3.9). T_{oxe} is usually determined from the inversion-region capacitance measured at $V_g = V_{dd}$. Quantization of states in the inversion layer causes the threshold voltage to increase beyond the prediction of the basic threshold voltage theory.

A **CCD (charge–coupled device)** is an imaging device based on an array of MOS capacitors operating under the **deep-depletion** condition, starved of inversion charge. Photo-generated carriers are collected in the surface potential wells, and the collected charge packets are transferred in a serial manner to the charge-sensing circuit located at the edge of the array. CCD imagers have been replaced by **CMOS imagers** where cost, size, and power consumption are more important than the best image quality. CMOS imagers integrate a charge-to-voltage conversion circuit in each sensing array element. In both types of imagers, color sensing is achieved with separate sensing elements for red, green, and blue in each pixel.

• PROBLEMS •

• Energy Band Diagram •

5.1 Sketch the energy band diagrams of an MOS capacitor with N-type silicon substrate and N^+ poly-Si gate at flatband, in accumulation, in depletion, at threshold, and in inversion.

5.2 Sketch the energy band diagrams (i) at thermal equilibrium and (ii) at flat band for the following MOS systems. Use a work function value that you find from any source.

(a) Tungsten, W, gate with 1 Ωcm N-type silicon substrate.

(b) Tungsten, W, gate with 1 Ωcm P-type silicon substrate.

(c) Heavily doped P^+ polycrystalline silicon gate with 1 Ωcm N-type silicon substrate.

(d) Heavily doped N^+-polycrystalline silicon gate with 1 Ωcm P-type silicon substrate.

● MOS System: Inversion, Threshold, Depletion, and Accumulation ●

5.3 The body of an MOS capacitor is N type. Match the "charge" diagrams (1) through (5) in Fig. 5–35 to (a) flat band, (b) accumulation, (c) depletion, (d) threshold, and (e) inversion.

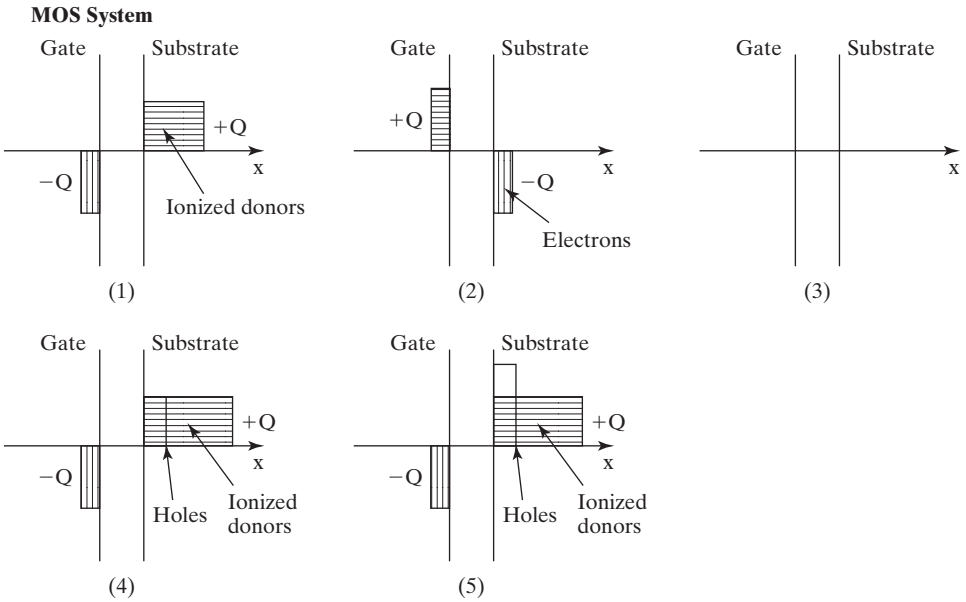

FIGURE 5–35

5.4 Consider an ideal MOS capacitor fabricated on a P-type silicon with a doping of $N_a = 5 \times 10^{16}\text{cm}^{-3}$ with an oxide thickness of 2 nm and an N^+ poly-gate.

(a) What is the flat-band voltage, V_{fb}, of this capacitor?

(b) Calculate the maximum depletion region width, W_{dmax}.

(c) Find the threshold voltage, V_t, of this device.

(d) If the gate is changed to P^+ poly, what would the threshold voltage be now?

5.5 Figure 5–36 shows the total charge per unit area in the P-type Si as a function of V_g for an MOS capacitor at 300 K.

(a) What is the oxide thickness?

(b) What is the doping concentration in Si?

(c) Find the voltage drop in oxide (V_{ox}) when $V_g - V_{fb} = -1$ V.

(d) Find the band bending in Si when $V_g - V_{fb} = 0.5$ V.

5.6 Make a series of qualitative sketches paralleling Figs. 5–11 to 5–14 (ϕ_s, W_{dep}, and charge as function of V_g) for an MOS capacitor having an N-type substrate and P^+poly gate. (Hint: At $V_g = V_t$, ϕ_s is negative. You may assume that V_t is negative.)

5.7 **(a)** Solve Eq. (5.3.1) for ϕ_s as a function of V_g.

(b) Find an expression for V_{ox} as a function of V_g.

(c) Make a rough sketch of ϕ_s vs. V_g and V_{ox} vs. V_g for $-3\text{ V} < V_g < 2\text{ V}$, $V_{fb} = -0.9$ V, $N_a = 10^{17}\text{cm}^{-3}$, and $T_{ox} = 3$ nm.

(d) Find W_{dep} as a function of V_g.

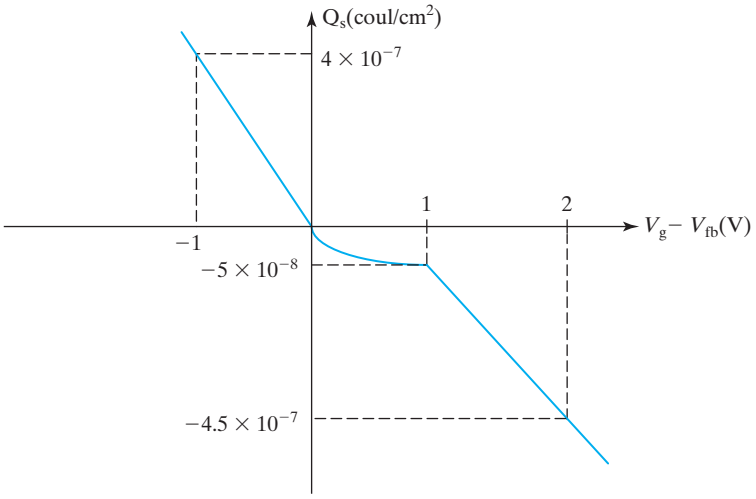

FIGURE 5–36

5.8 Consider an MOS capacitor fabricated on P-type Si substrate with a doping of 5×10^{16} cm^{-3} with oxide thickness of 10nm and N^+ poly-gate.

(a) Find C_{ox}, V_{fb}, and V_t.

(b) Find the accumulation charge (C/cm^2) at $V_g = V_{fb} - 1$ V.

(c) Find the depletion and inversion charge at $V_g = 2$ V.

(d) Plot the total substrate charge as a function of V_g for V_g from –2 to 2 V.

5.9 If we decrease the substrate doping concentration, how will the following parameters be affected? (Please indicate your answer by putting a mark, X, in the correct column.) Write down any relevant equation and explain briefly how you obtain the answer (a few words or one sentence). Assume the gate material is N^+poly and the body is P type.

	Parameters	Increase	Decrease	Unchanged
A	Accumulation region capacitance			
B	Flat-band voltage, V_{fb}			
C	Depletion-region capacitance			
D	Threshold voltage, V_t			
E	Inversion region capacitance			

5.10 From the high-frequency *C–V* measurements on an MOS capacitor with P-Si substrate performed at 300 K, the following characteristics were deduced:

Oxide thickness = 30 nm
Substrate doping = 10^{16} cm^{-3}
Flat-band voltage = –2 V

Construct the *C–V* curve, labeling everything, including the values of the oxide capacitance, flat-band voltage, and threshold voltage. Assuming an Al gate with 4.1 V work function, compute the effective oxide charge.

● Field Threshold Voltage ●

5.11 Metal interconnect lines in IC circuits form parasitic MOS capacitors as illustrated in Fig. 5–37. Generally, one wants to prevent the underlying Si substrate from becoming inverted. Otherwise, parasitic transistors may be formed and create undesirable current paths between the N^+ diffusions.

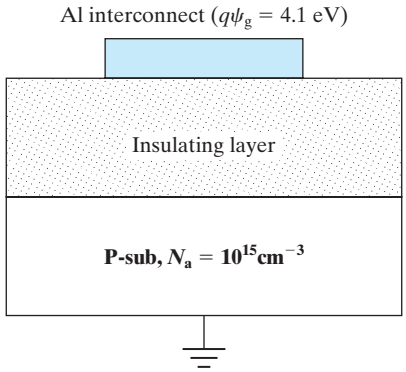

FIGURE 5–37

(a) Find V_{fb} of this parasitic MOS capacitor.

(b) If the interconnect voltage can be as high as 5 V, what is the maximum capacitance (F/cm^2) of the insulating layer that can be tolerated without forming an inversion layer?

(c) If the insulating layer thickness must be 1 μm for fabrication considerations, what should the dielectric constant $K = \varepsilon/\varepsilon_0$ of the insulating material be to make $V_t = 5$ V?

(d) Is the answer in (c) the minimum or maximum allowable K to prevent inversion?

(e) At $V_g = V_t + 2$ V ($V_t = 5$ V), what is the area charge density (C/cm^2) in the inversion layer?

(f) At $V_g = V_t = 5$ V, what is the high-frequency MOS capacitance (F/cm^2)?

(g) At $V_g = V_t + 2$ V ($V_t = 5$ V), what voltage is dropped across the insulating layer?

● Oxide Charge ●

5.12 Consider the C–V curve of an MOS capacitor in Fig. 5–38 (the solid line). The capacitor area is 6,400 μm^2. $C_0 = 45$ pF and $C_1 = 5.6$ pF.

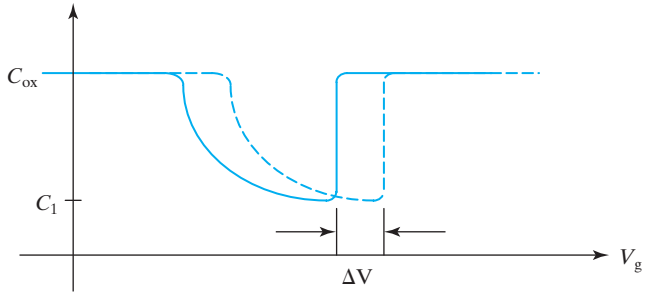

FIGURE 5–38

If, due to the oxide fixed charge, the *C–V* curve is shifted from the solid line to the dashed line with $\Delta V = 0.05$ V, what is the charge polarity and the area density (C/cm^2) of the oxide fixed charge?

5.13 Why is oxide charge undesirable? How do mobile charges get introduced into the oxide? How can this problem be overcome?

● C–V Characteristics ●

5.14 Derive $C(V_g)$ in Eq. (5.6.4). [Hint: Solve Eq. (5.3.3) for W_{dep}.]

5.15 Answer the following questions based on the *C–V* curve for an MOS capacitor shown in Fig. 5–39. The area of the capacitor is 10^4 μm^2.

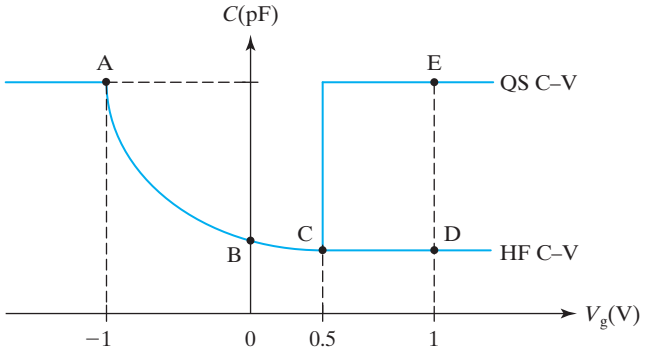

FIGURE 5–39

(a) Is the substrate doping N type or P type?

(b) What is the thickness of the oxide in the MOS capacitor?

(c) What is the doping concentration of the substrate, N_{sub}?

(d) What is the value of the capacitance at position C on the *C–V* curve shown above?

(e) Sketch the energy band diagram of the MOS structure at positions A, B, C, D, and E on the *C–V* curve.

(f) At location B on the *C–V* curve, what is the band bending, ϕ_s?

5.16 The C–V characteristics of MOS capacitors A (solid line) and B (dashed line), both having the same area, are shown in Fig. 5–40.

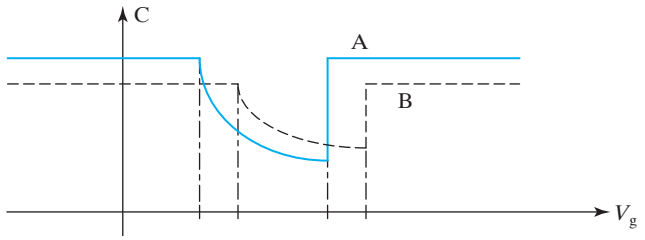

FIGURE 5–40

(a) Are the substrate P type or N type? How do you know this?

(b) Circle A or B to select the capacitor having larger

X_{ox}: A B

V_{fb}: A B

X_{dmax}: A B

N_{sub}: A B

V_t: A B

5.17 Compare the maximum capacitance that can be achieved in an area $100 \times 100\ \mu m^2$ by using either an MOS capacitor or a reverse-biased P^+N junction diode. Assume an oxide breakdown field of 8×10^6 V/cm, a 5V operating voltage, and a safety factor of two (i.e., design the MOS oxide for 10 V breakdown). The P^+N junction is built by diffusing boron into N-type silicon doped to $10^{16}\ cm^{-3}$

5.18 Consider the silicon–oxide–silicon structure shown in Fig. 5–41. Both silicon regions are N type with uniform doping of $N_d = 10^{16}\ cm^{-3}$.

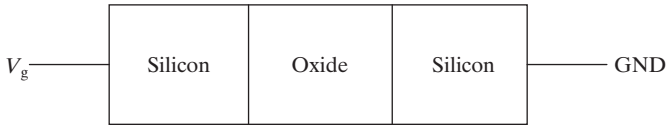

FIGURE 5–41

(a) What would be the flat-band voltage for this structure? Draw the energy band diagram for the structure for (i) $V_g = 0$, (ii) $V_g < 0$ and large, and (iii) $V_g > 0$ and large.

(b) Sketch the expected shape of the high-frequency C–V characteristics for the structure. What are the values of the capacitance for large positive and large negative V_g?

(c) If silicon on the left-hand side in the figure above is P-type doped with $N_a = 10^{16}\ cm^{-3}$, sketch the C–V characteristics for the new structure.

5.19 Fill in the following table with appropriate mathematical expressions using the basic MOS C–V theory.

Bias condition	Surface potential	MOS capacitance (LF)	MOS capacitance (HF)	MOSFET capacitance
Accumulation				
Flat band				
Just below threshold				
Inversion				

5.20 The oxide thickness (T_{ox}) and the doping concentration (N_a or N_d) of the silicon substrate can be determined using the high-frequency *C–V* data shown in Fig. 5–42 for an MOS structure.

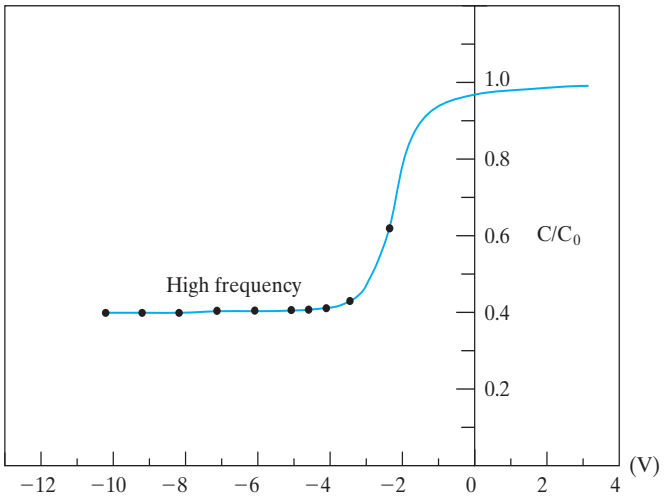

FIGURE 5–42

(a) Identify the regions of accumulation, depletion, and inversion in the substrate corresponding to this *C–V* curve. What is the doping type of the semiconductor?

(b) If the maximum capacitance of the structure C_0 (which is equal to $C_{ox} \times$ Area) is 82 pF and the gate area is 4.75×10^{-3} cm^2, what is the value of T_{ox}?

(c) Determine the concentration in the silicon substrate. Assume a uniform doping concentration.

(d) Assuming that the gate is P$^+$type, what is Q_{ox}?

● Poly-Gate Depletion ●

5.21 **(a)** Derive Eq. (5.8.1).

(b) Derive an expression for the voltage drop in the poly-depletion region, i.e., the band bending in the poly-Si gate, ϕ_s. Assume that the electric field inside the oxide, $\mathscr{E}_{ox}$, is known.

(c) Continue from (b) and express ϕ_{poly} in terms of V_g, not $\mathscr{E}_{ox}$. Assume surface inversion, i.e., $V_g > V_t$. Other usual MOS parameters such as V_{fb}, T_{ox}, and ϕ_B may also appear. Hint: $V_g = V_{fb} + V_{ox} + 2\phi_B + \phi_{poly}$.

(d) Using the result of (c), find an expression for W_{dpoly} in terms of V_g, not $\mathscr{E}_{ox}$.

For part (e), (f), and (g), assume $T_{ox} = 2$ nm, $N_a = 10^{17}$cm^{-3}, $N_d = 6 \times 10^{19}$ cm^{-3} (for N$^+$poly-gate), and $V_g = 1.5$ V.

(e) Evaluate ϕ_{poly} and W_{dpoly}.

(f) Calculate V_t using Eq. (5.4.3). (The poly-depletion effect maybe ignored in V_t calculation because $\mathscr{E}_{ox}$ is very low at $V_g = V_t$.) Then, using ϕ_{poly} from part (e) in Eq. (5.8.3), find Q_{inv}.

(g) Calculate $Q_{inv} = C_{oxe}(V_g - V_t)$ with C_{oxe} given by Eq. (5.8.2).

Discussion:
Equation (5.8.2) is correct for the small signal capacitance

$$C(V_g) = dQ(V_g)/dV_g \Rightarrow Q(V_g) = \int C(V_g)dV_g$$

Here, part (g) does not yield the correct Q_{inv} because it assumes a constant C_{oxe}. C_{oxe} varies with V_g due to the poly-depletion effect even for $V_g >; V_t$. The answer for part (f) is the correct value for Q_{inv}.

5.22 Draw an energy band diagram for Example 5–3 in Section 5.8. You need to decide whether V_g and V_{ox} are positive or negative. (Hint: The problem is about gate depletion.)

5.23 There is a voltage drop in the gate depletion region (V_{poly}). Express the following items using V_{poly}, the gate doping concentration N_{poly}, and the oxide capacitance C_{ox} as given variables.

(a) What is the charge density Q_{poly} in the gate depletion region?

(b) What is C_{poly}? ($C_{poly} = \varepsilon_s / W_{dpoly}$)

(c) What is the total MOS capacitance in the inversion region when poly depletion is included?

● Threshold Voltage Expression ●

5.24 After studying the derivation of Eq. (5.4.3), write down the steps of derivation on your own.

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